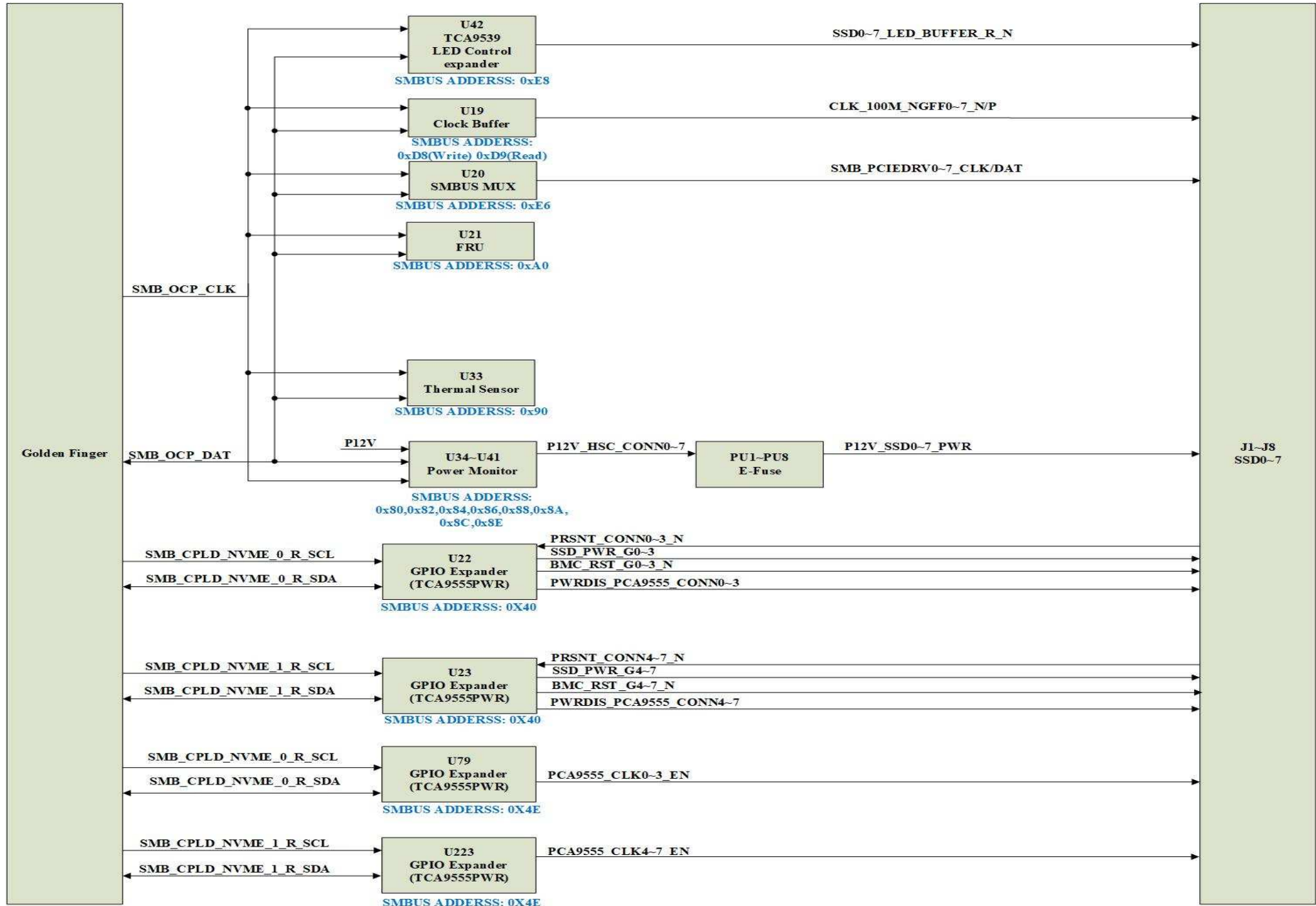


FOCE IOX E1.S Board_TI

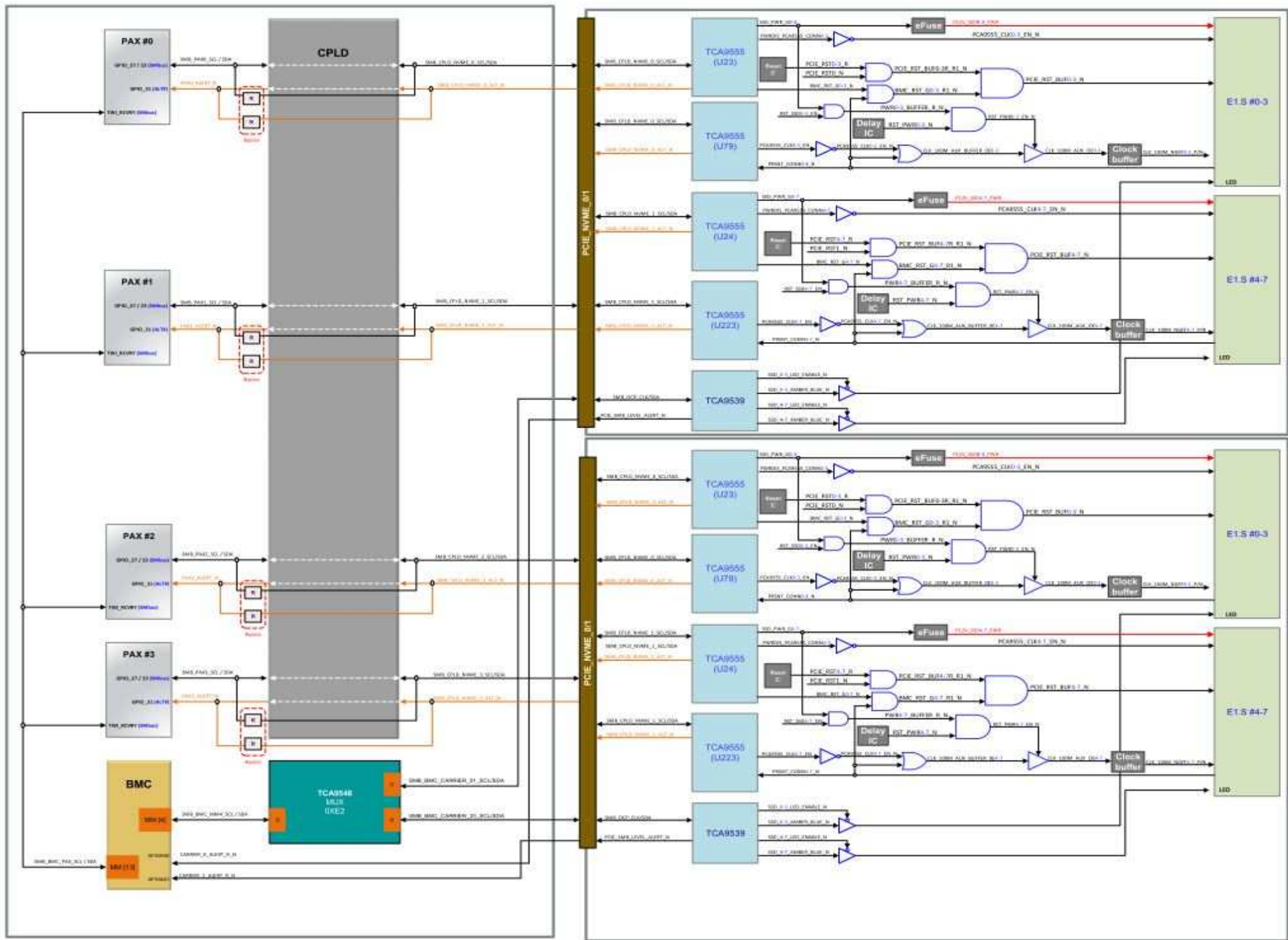
PCB REV: C
PCBA REV:
SCH Rev: V01
LAST UPDAE: 2021/07/01

INDEX

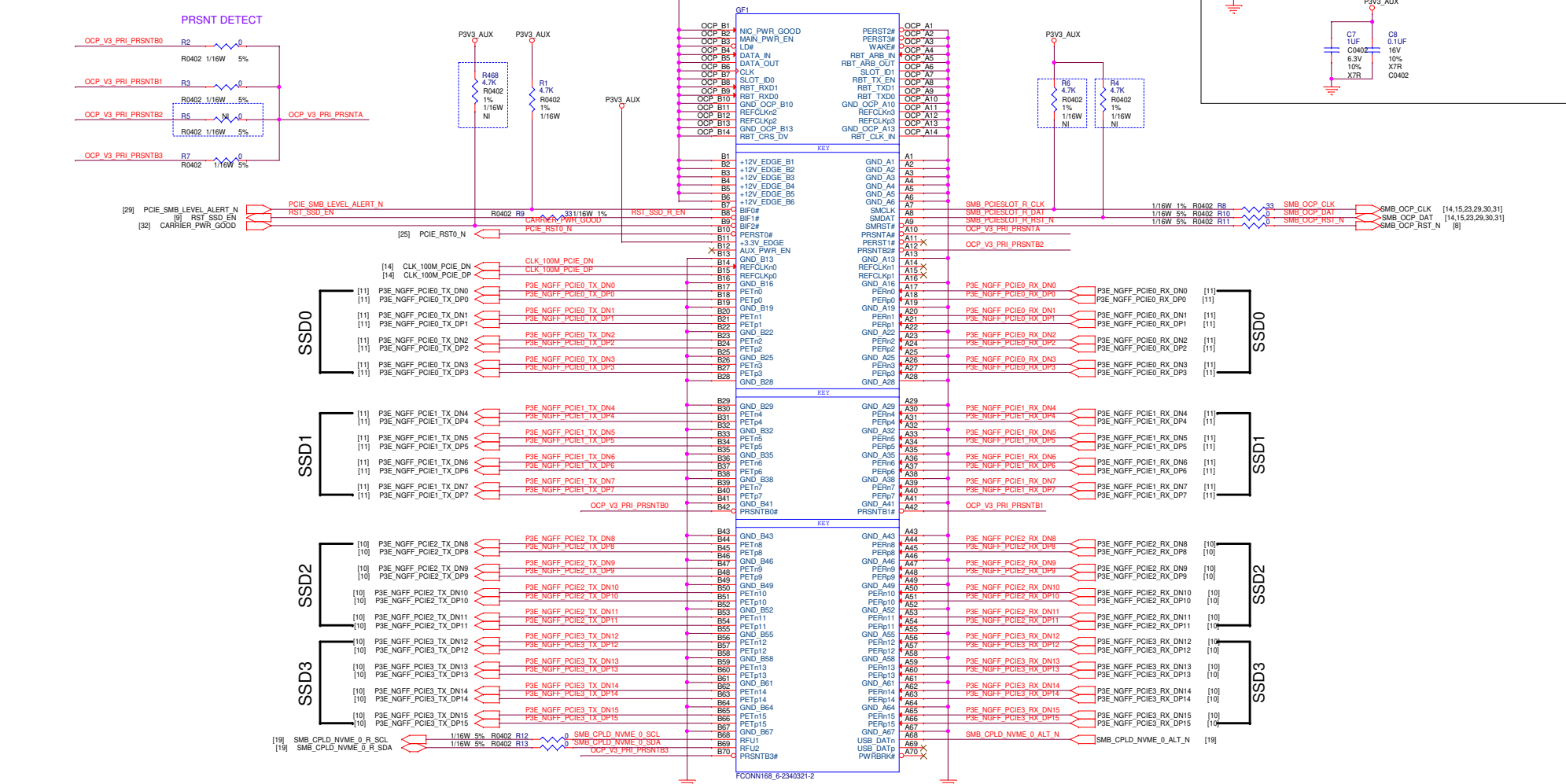
- 1 Cover Page
- 2 Page Index
- 3 Block Diagram
- 4 SSD HSC Diagram
- 5 Primary Gold Finger
- 6 Secondary Gold Finger
- 7 Enable Circuit
- 8 Reset Circuit
- 9 Reset Circuit2
- 10 SSD Slot0/1
- 11 SSD Slot2/3
- 12 SSD Slot4/5
- 13 SSD Slot6/7
- 14 Clock Buffer
- 15 SMBus MUX
- 16 Clock Control Circuit
- 17 BLANK
- 18 BLANK
- 19 TCA9555
- 20 Buffer Circuit
- 21 TCA9555 PWRDIS
- 22 12V E-fuse
- 23 SSD LED Control
- 24 3.3V E-fuse
- 25 PCIE SSD Reset Circuit
- 26 RESET CIRCUIT1
- 27 RESET CIRCUIT2
- 28 TCA9555 CLOCK CIRCUIT
- 29 Thermal Sensor
- 30 POWER MONITOR1
- 31 POWER MONITOR2
- 32 SSD PG Circuit
- 33 Dummy Symbol
- 34 Loss Coupon
- 35 SCREW HOLE



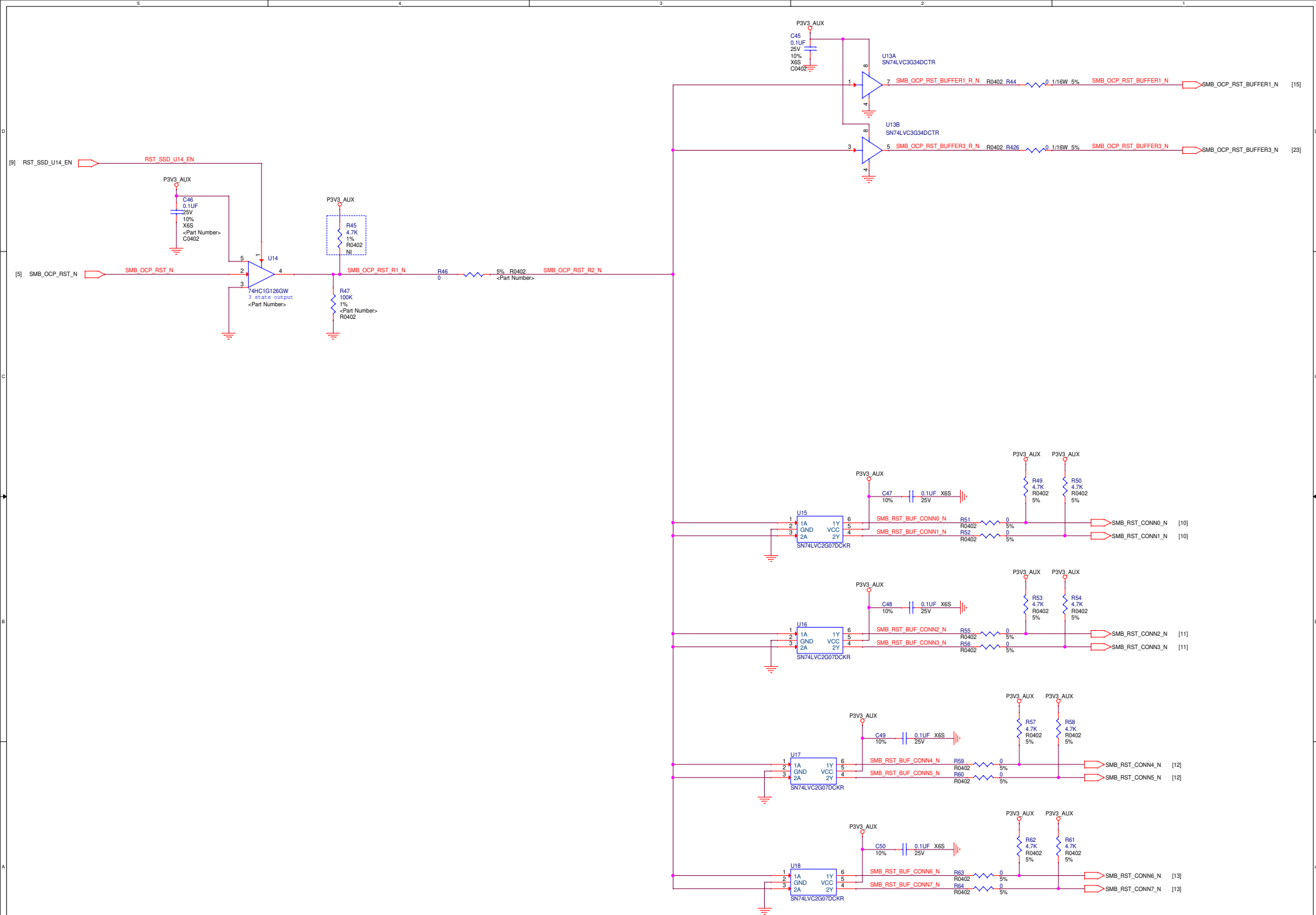
Block Diagram



SKU	PRSNBT0	PRSNBT1	PRSNBT2	PRSNBT3	ID Register
M.2	1	1	0	0	0xCC
E1.S.FAB.1	0	1	0	0	0x44
E1.S.FAB.2/3(T1)	0	0	1	0	0x22
M.2(Re-spin)	1	1	0	1	0xDD
E1.S.FAB.3(MPS)	0	0	1	1	0x33

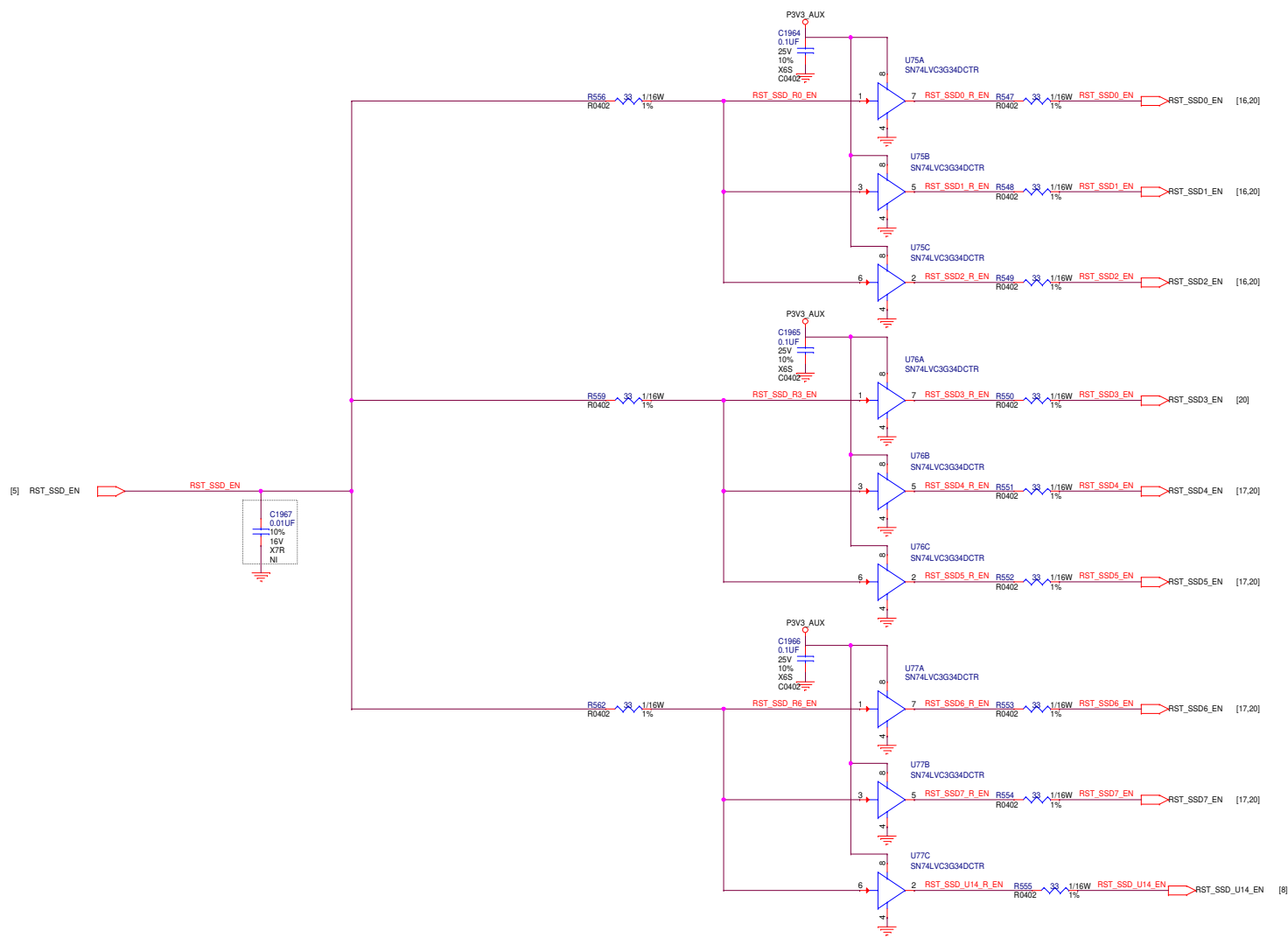






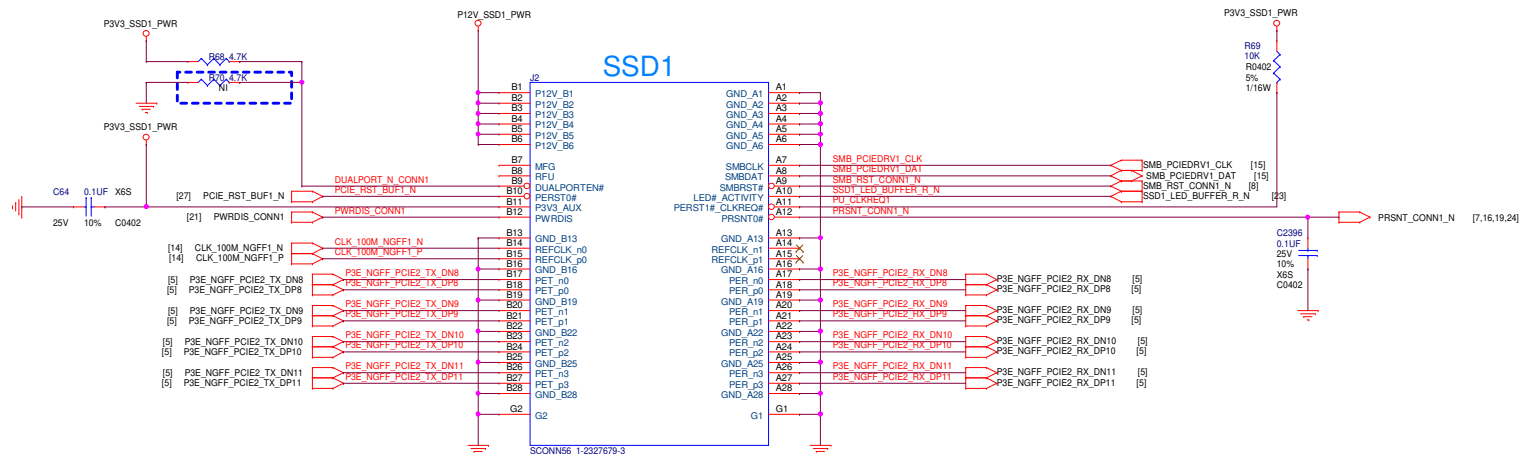
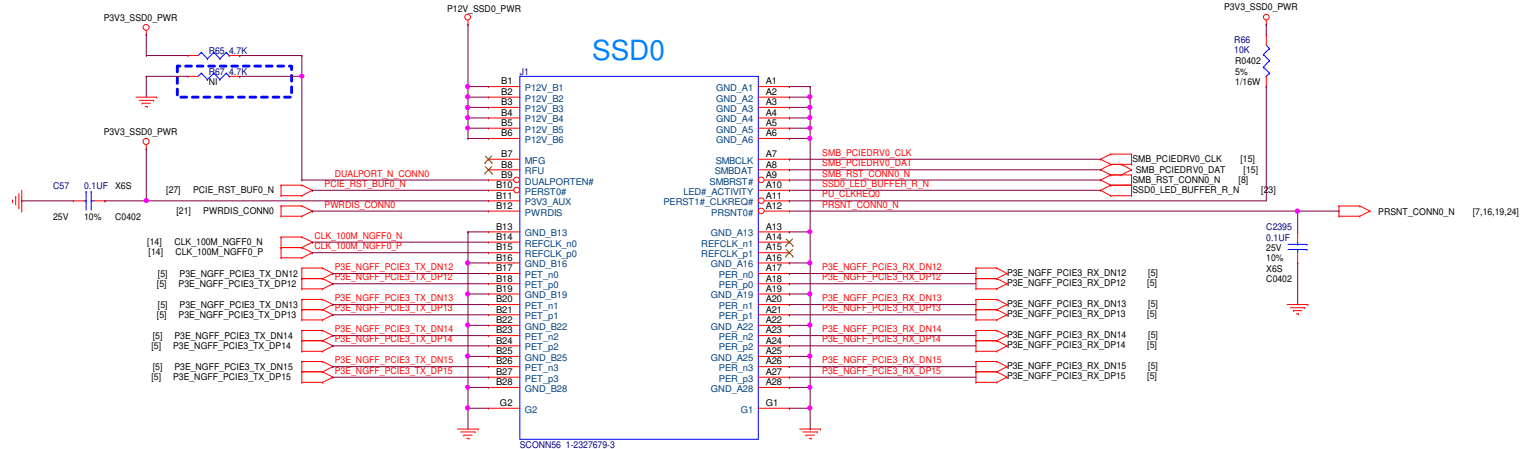
Reset Circuit

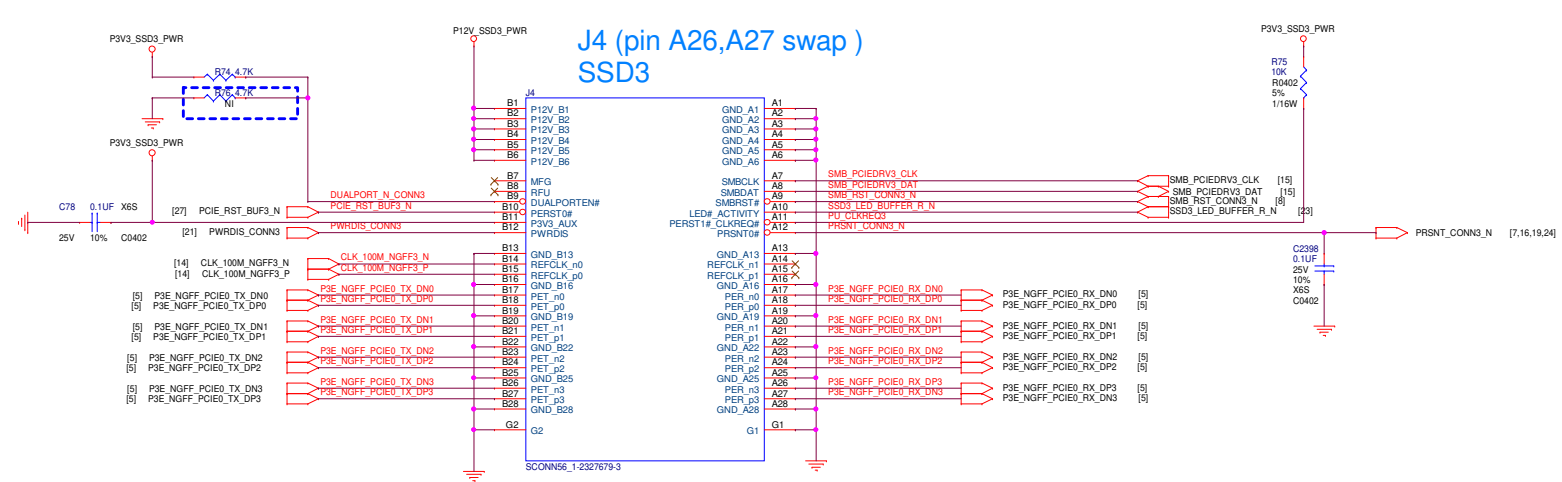
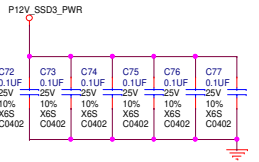
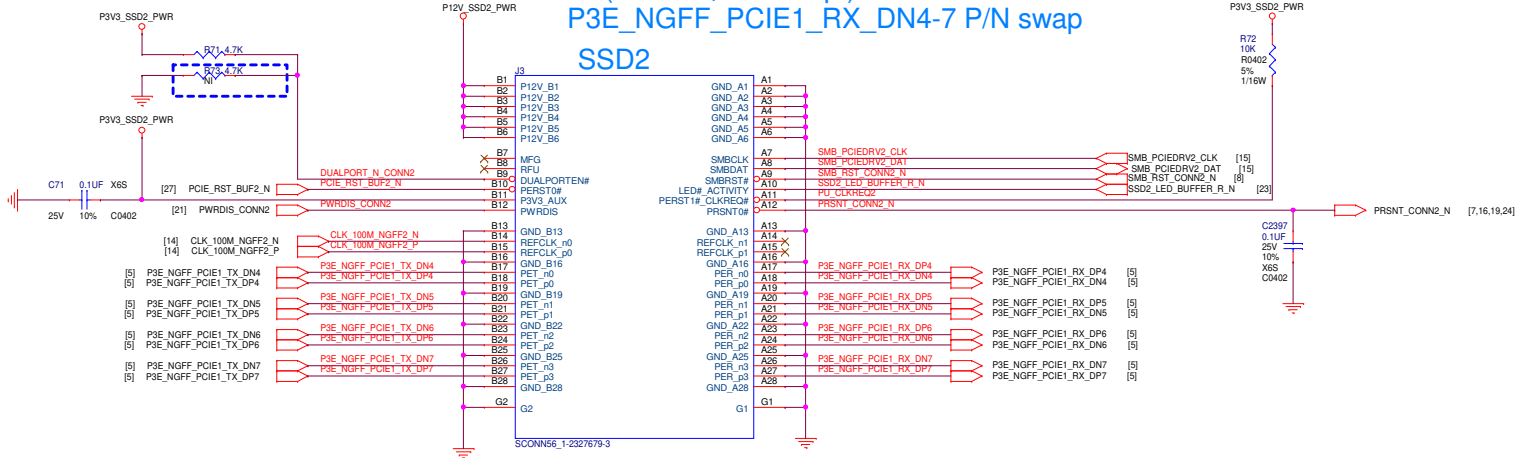
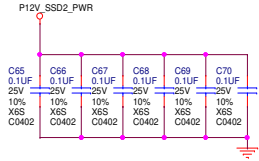
5 4 3 2 1

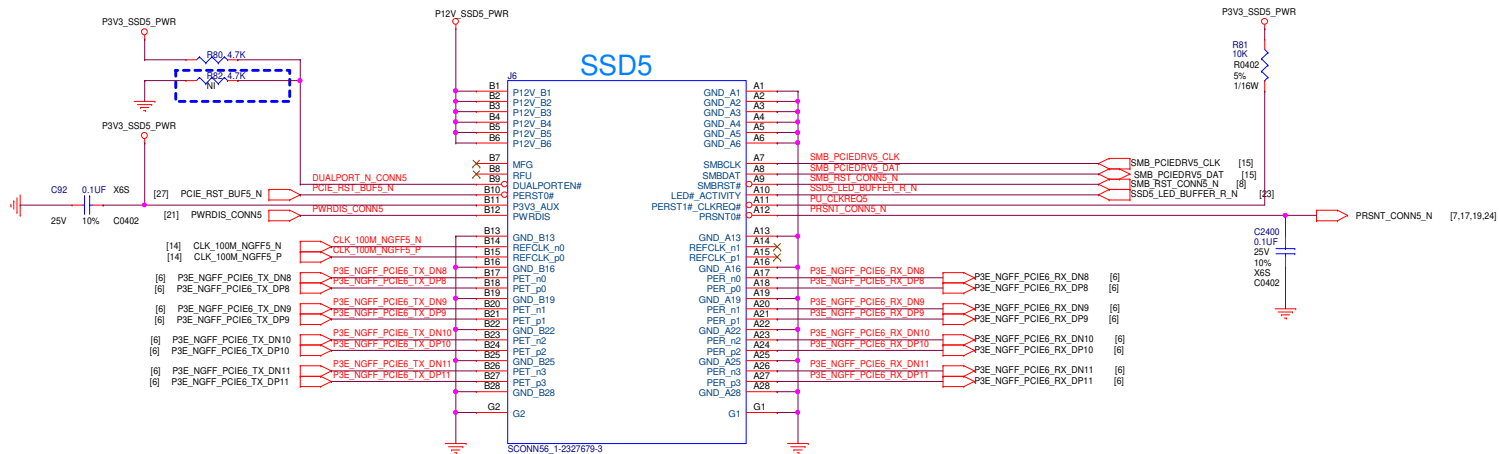
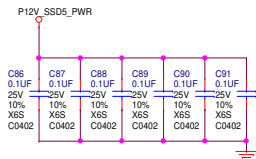
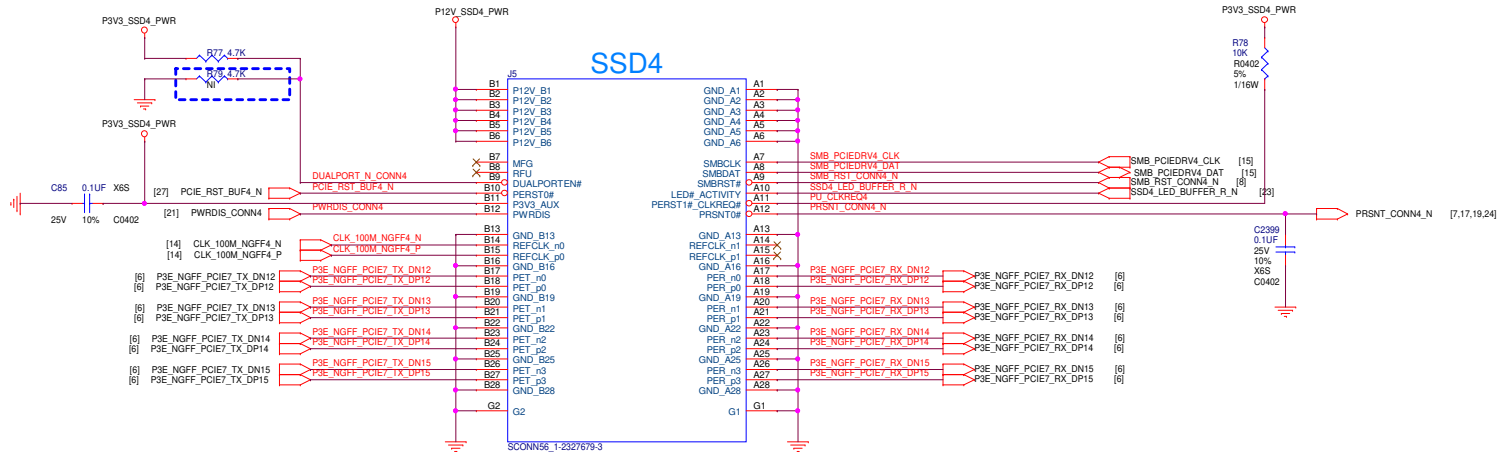
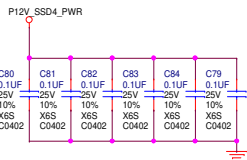


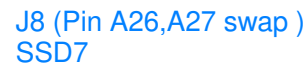
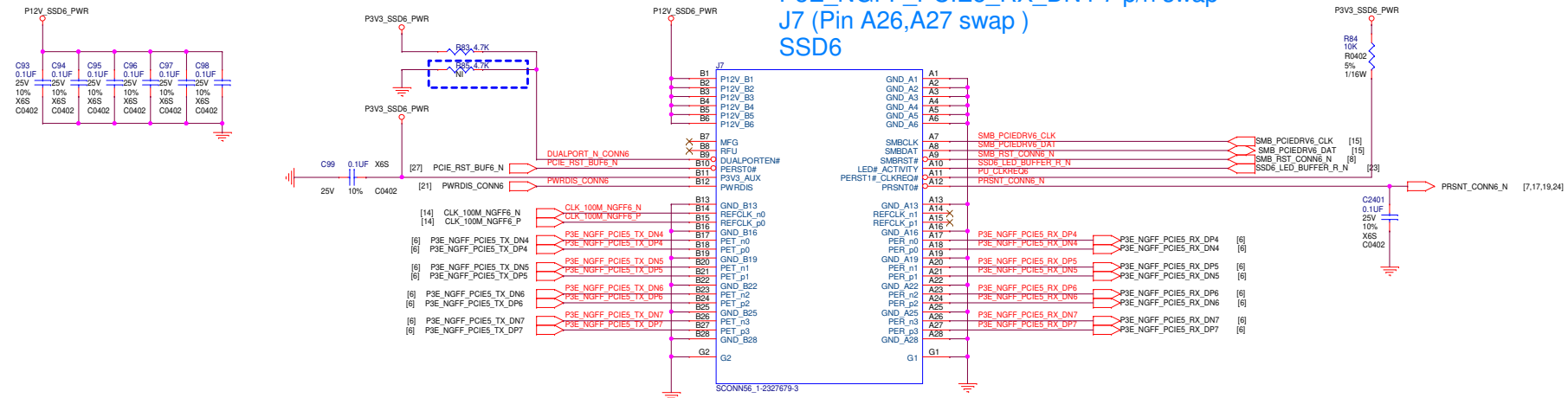
5 4 3 2 1

Reset Circuit









PLL Operating Mode Table

HiBW_BypM_LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

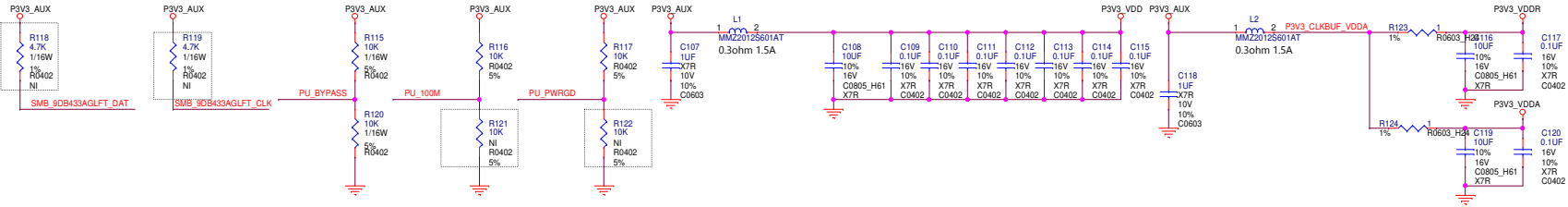
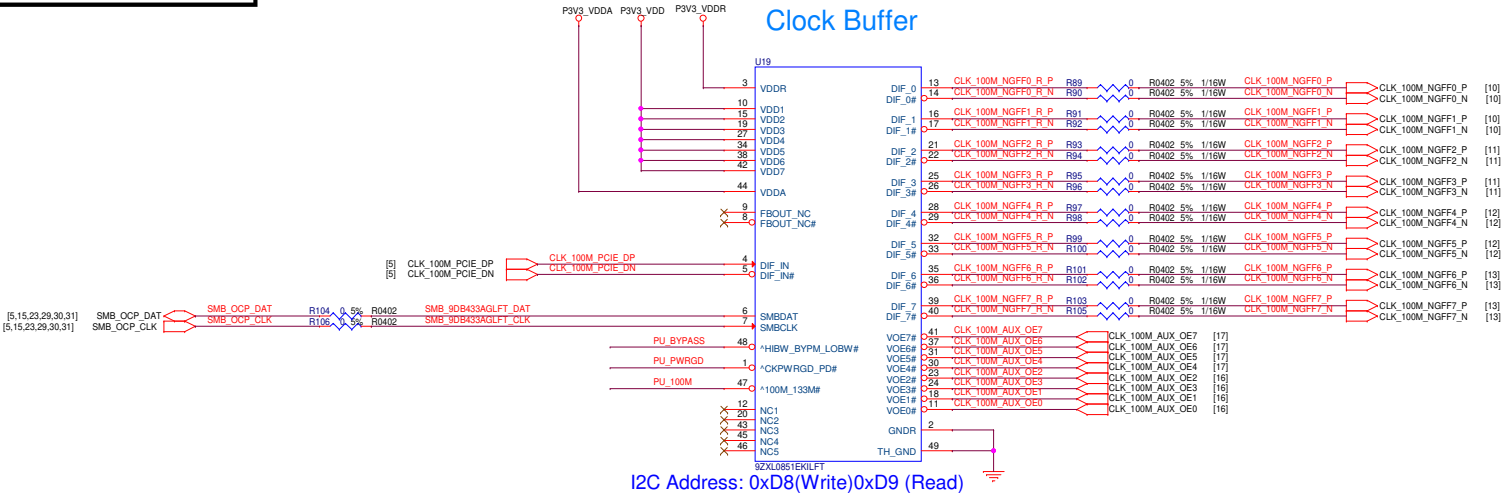
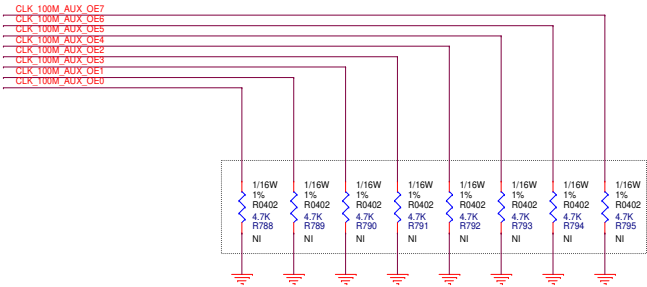
NOTE: PLL is OFF in Bypass Mode

PLL Operating Mode Readback Table

HiBW_BypM_LoBW#	Byte0, bit 7	Byte 0, bit 6
Low (Low BW)	0	0
Mid (Bypass)	0	1
High (High BW)	1	1

SMBus Address

Address	+ Read/Write bit
1101100	x



Clock Buffer

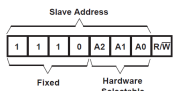
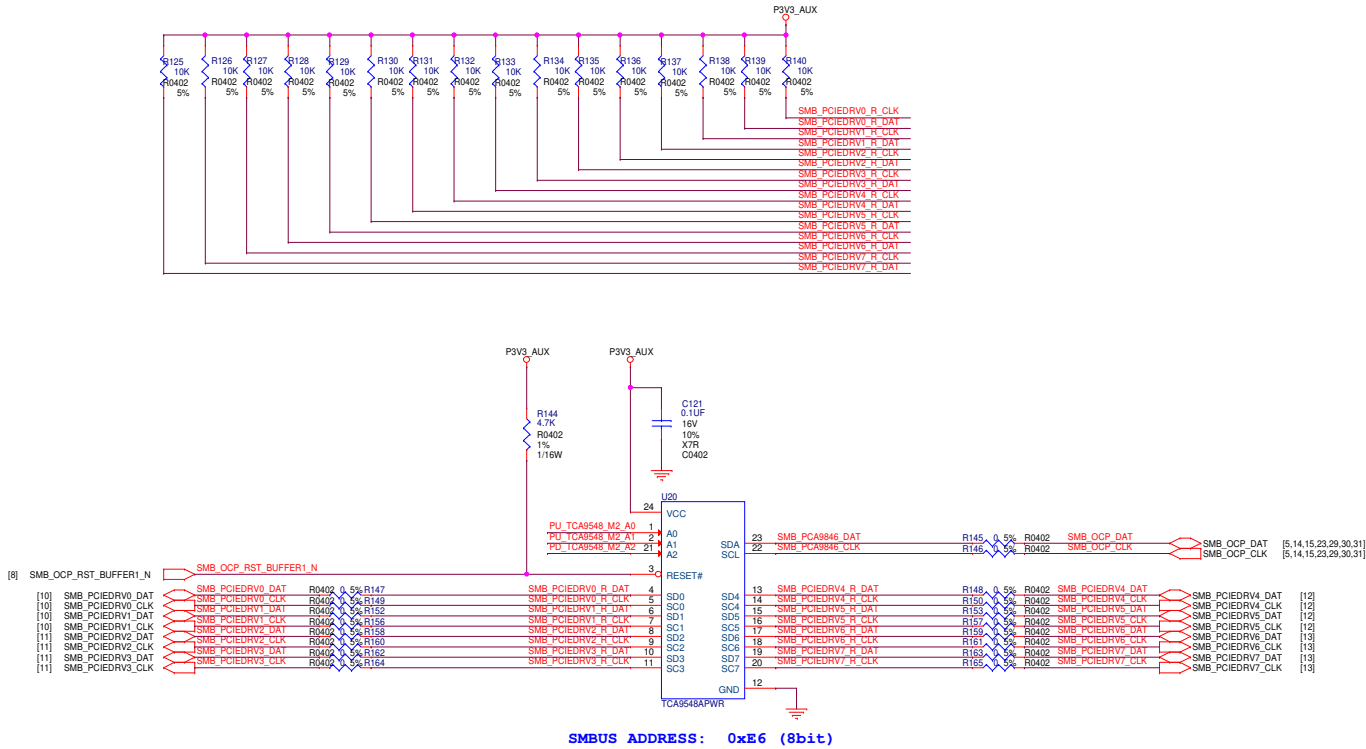
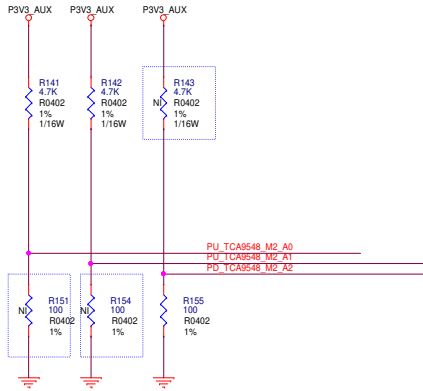


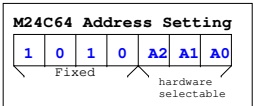
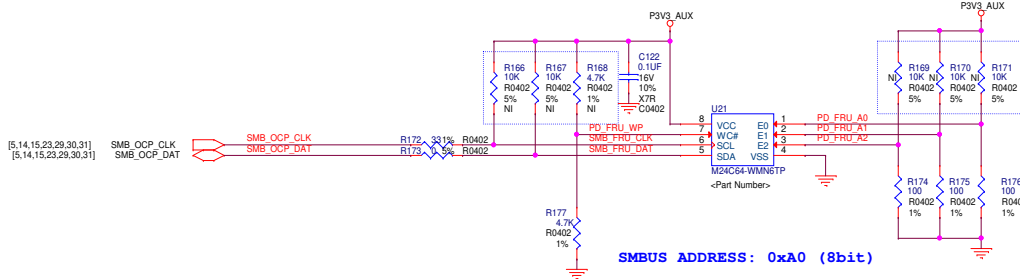
Figure 4. TCA9548A Address

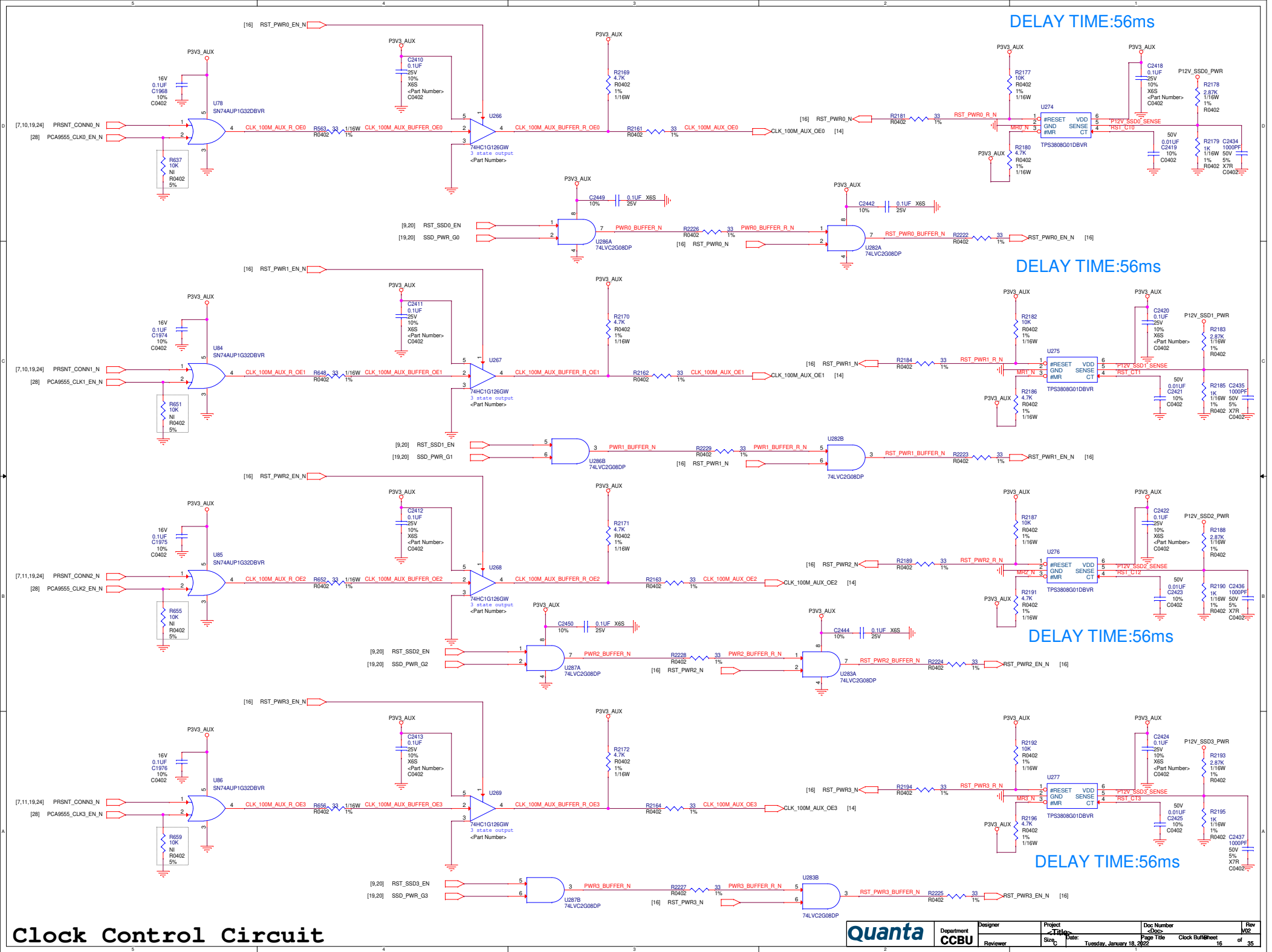
Table 1. Address Reference

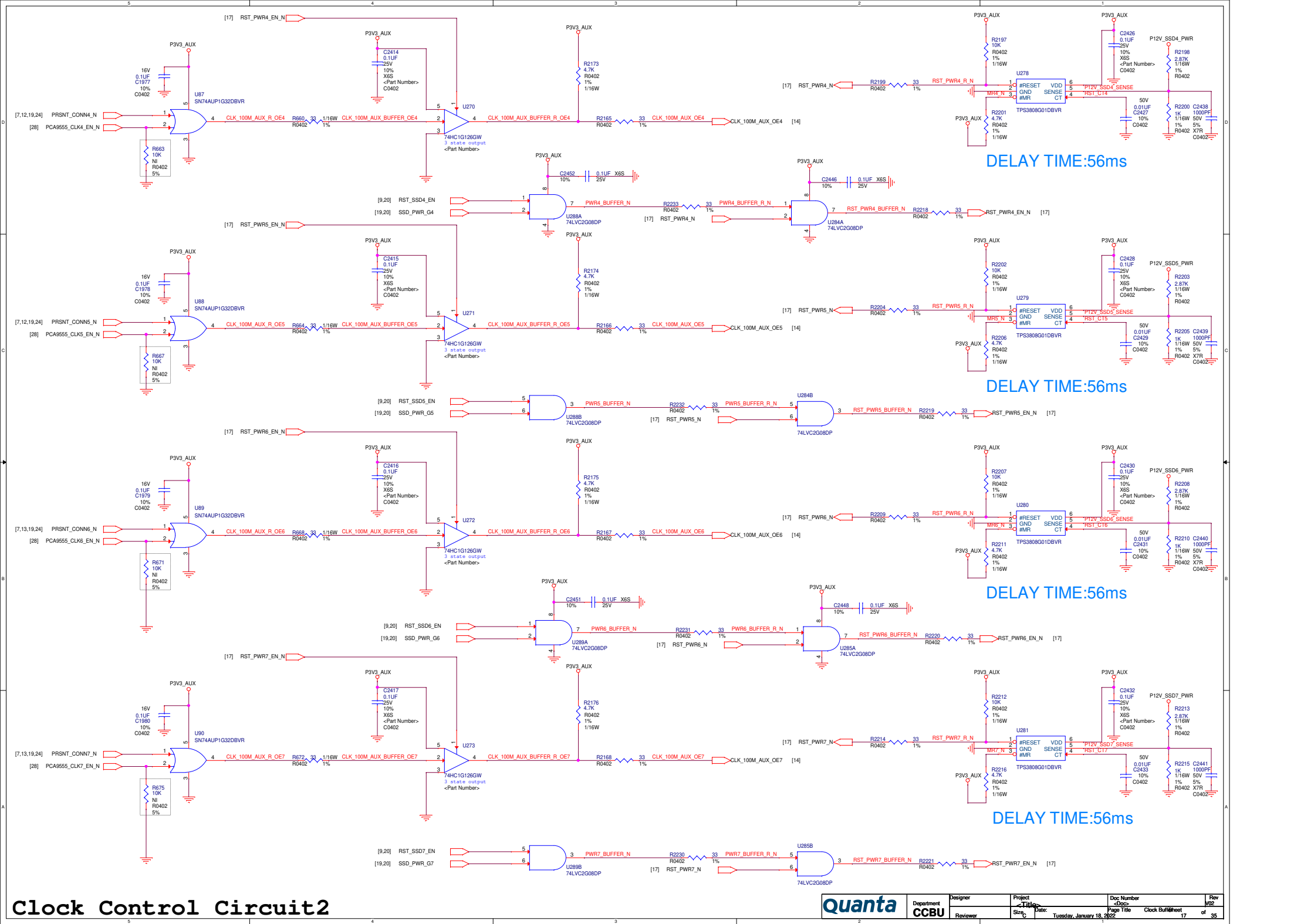
INPUTS			I ² C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)



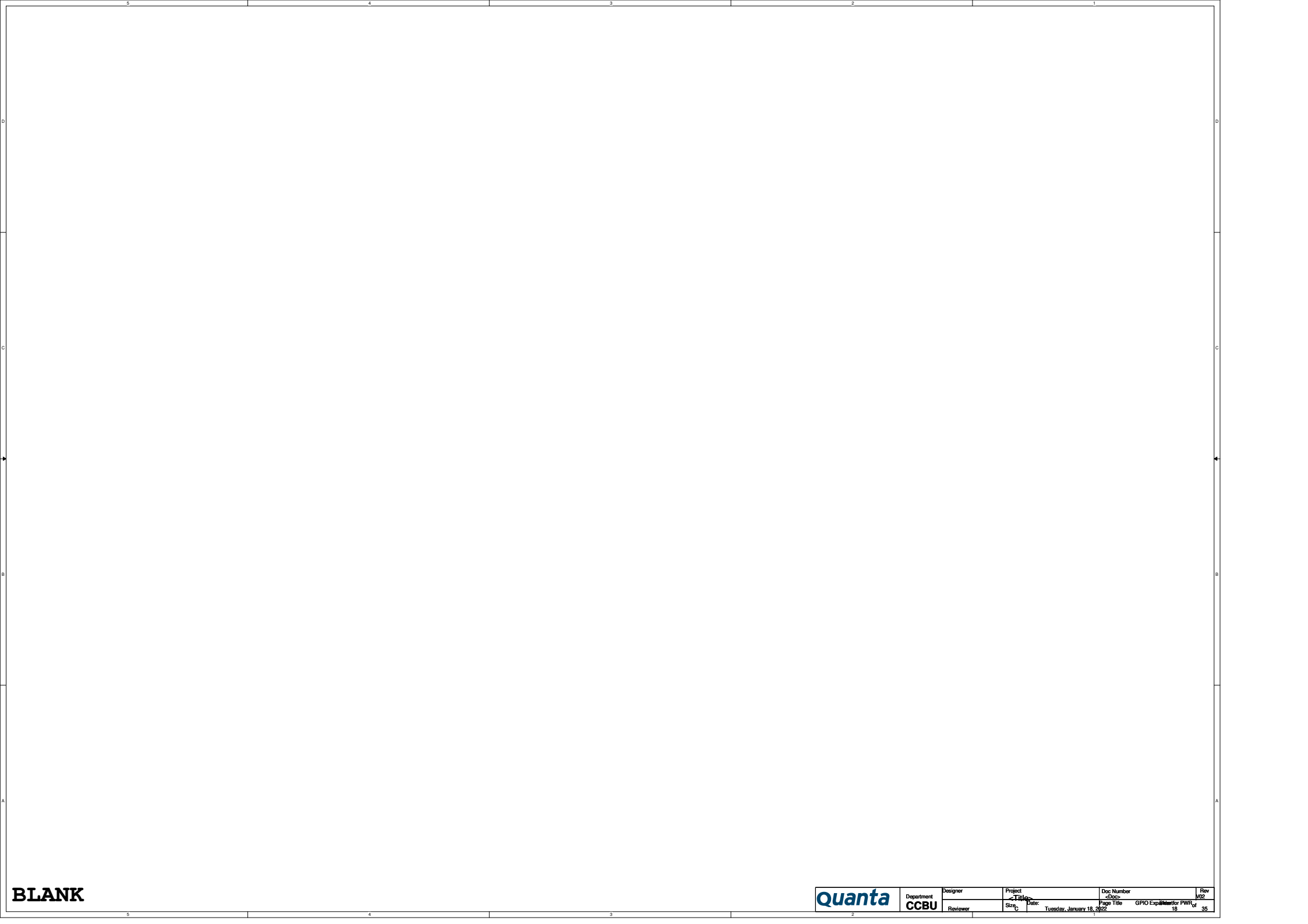
FRU





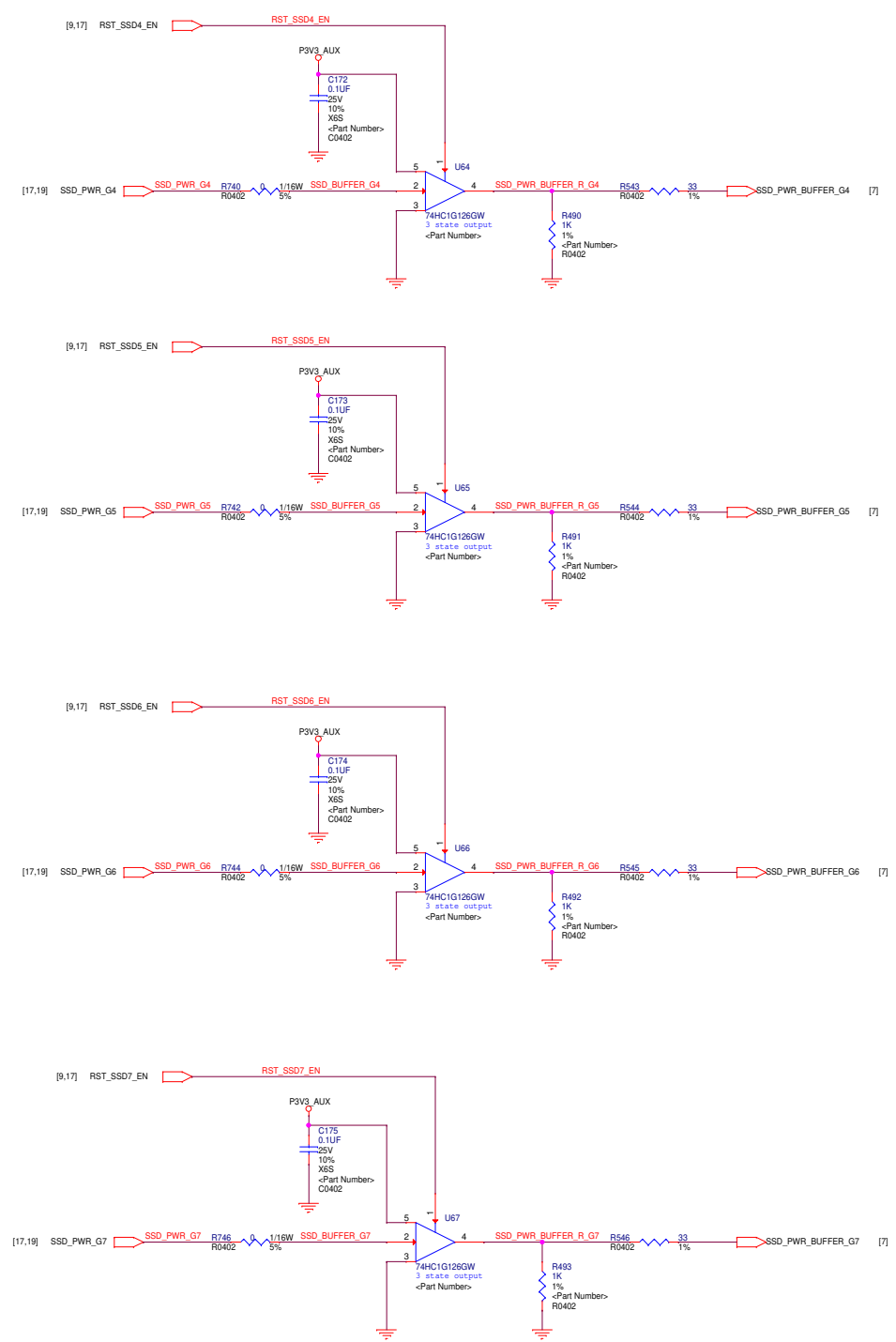
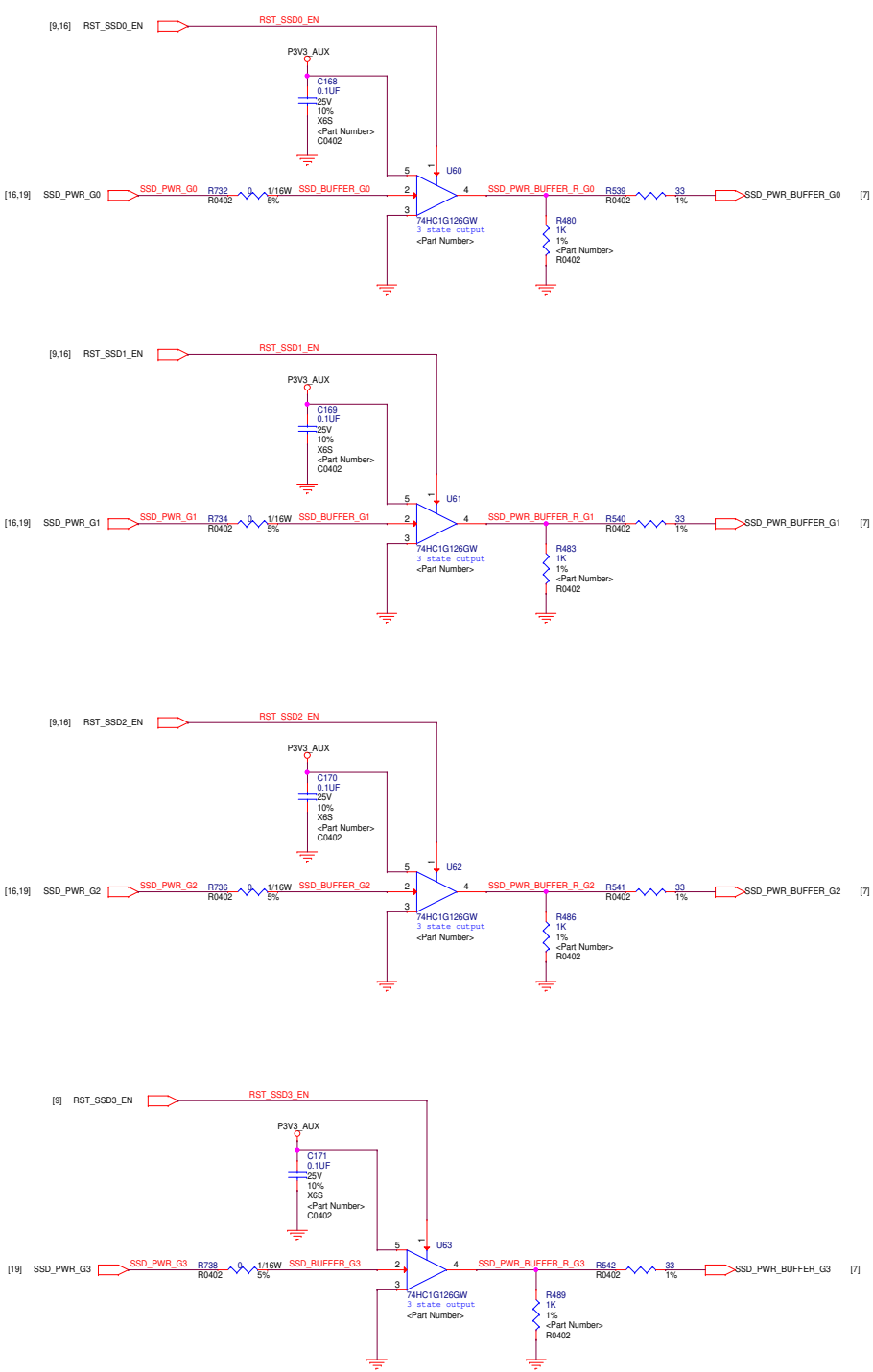


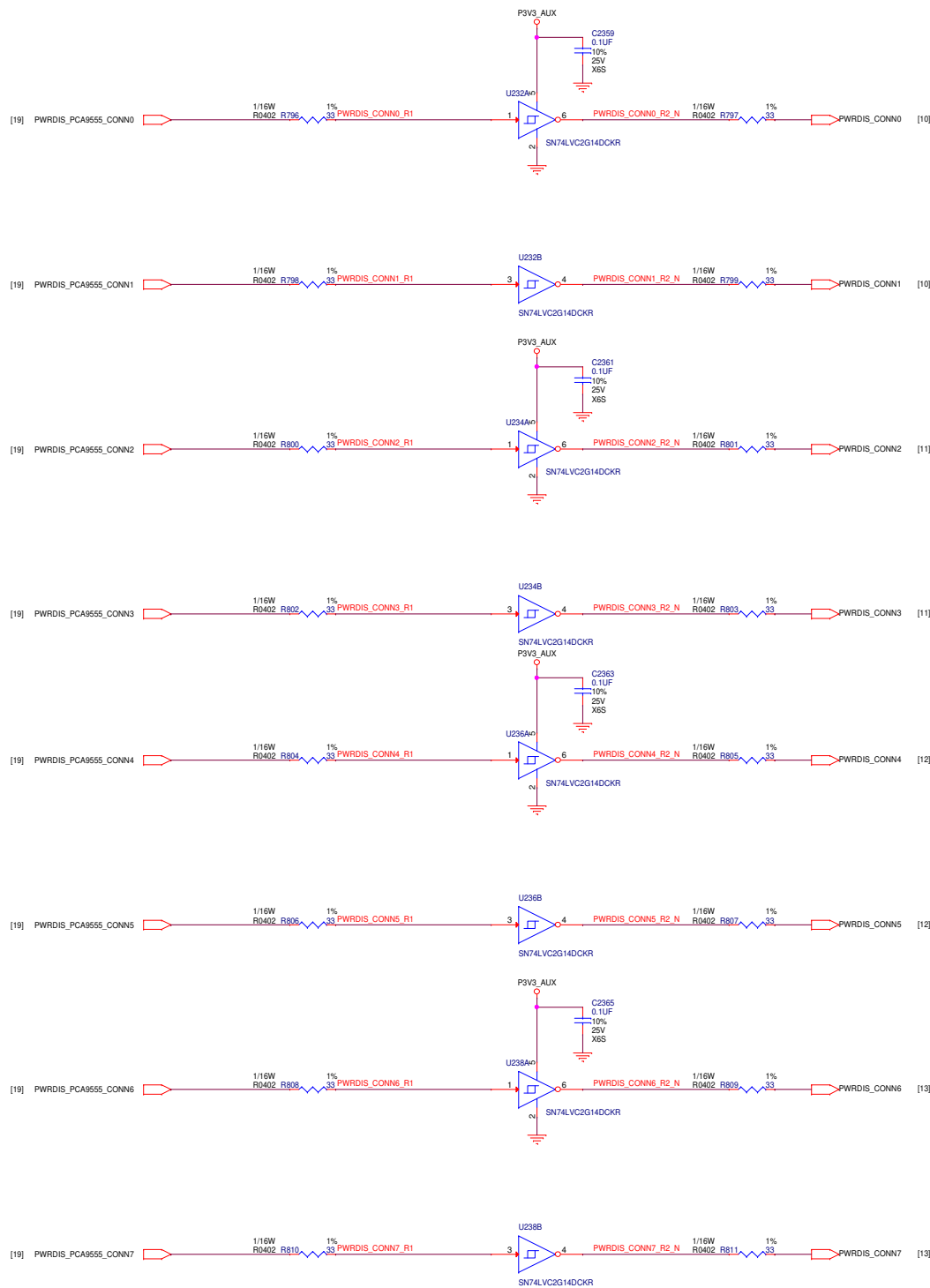
Clock Control Circuit2



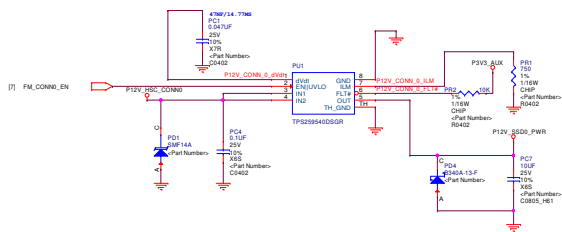
BLANK

Buffer Circuit

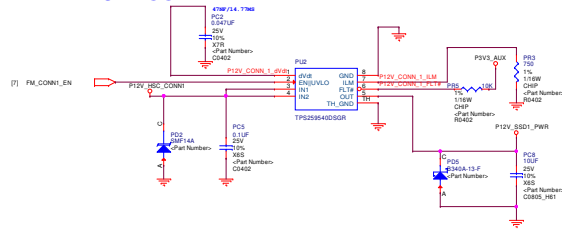




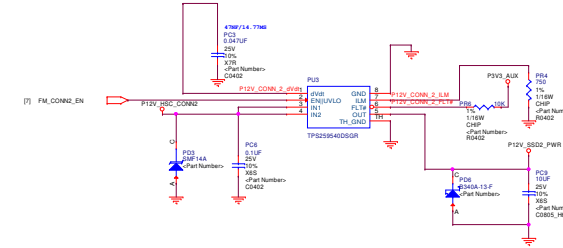
PWR for SSD0



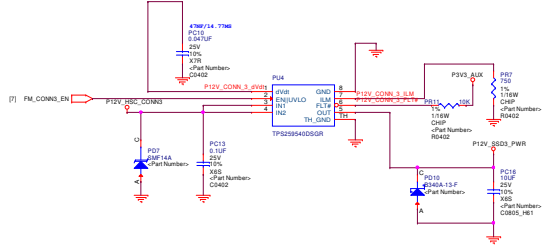
PWR for SSD1



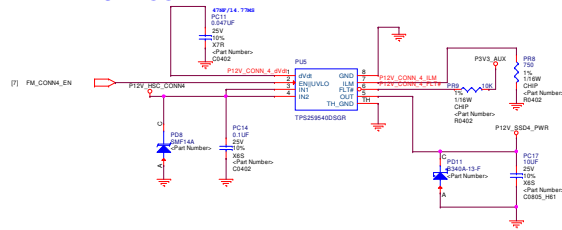
PWR for SSD2



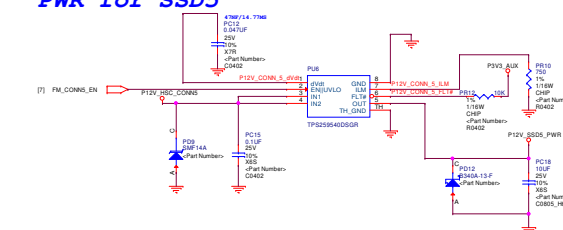
PWR for SSD3



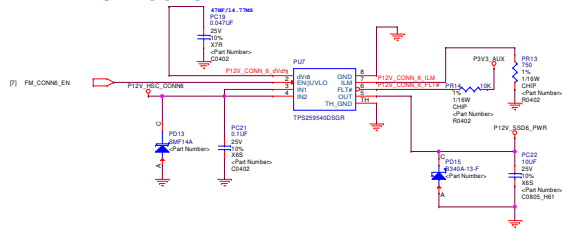
PWR for SSD4



PWR for SSD5



PWR for SSD6



PWR for SSD7

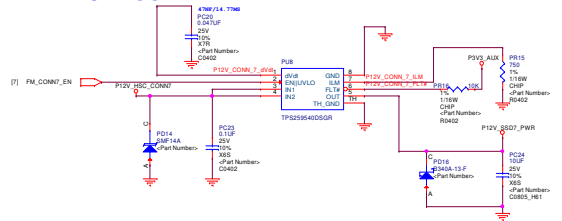
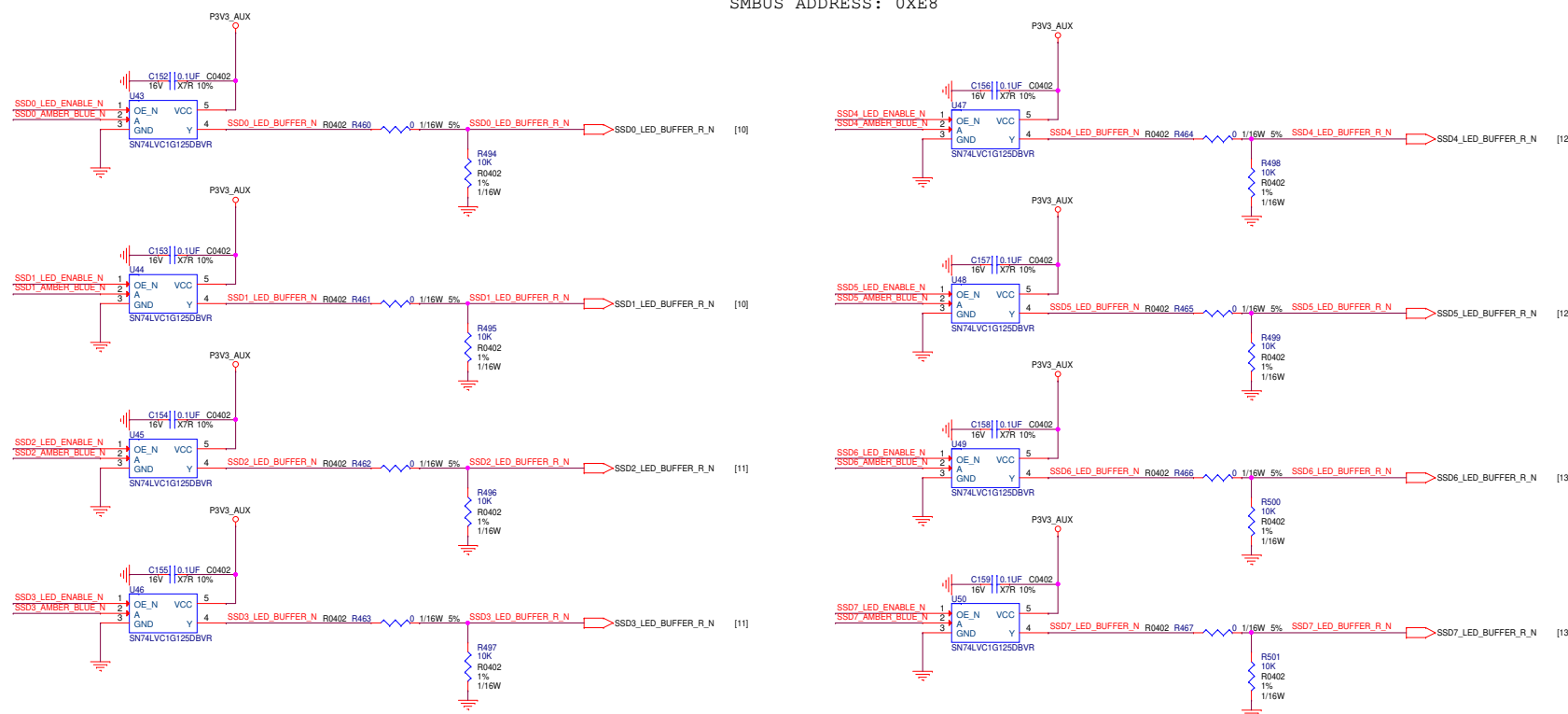
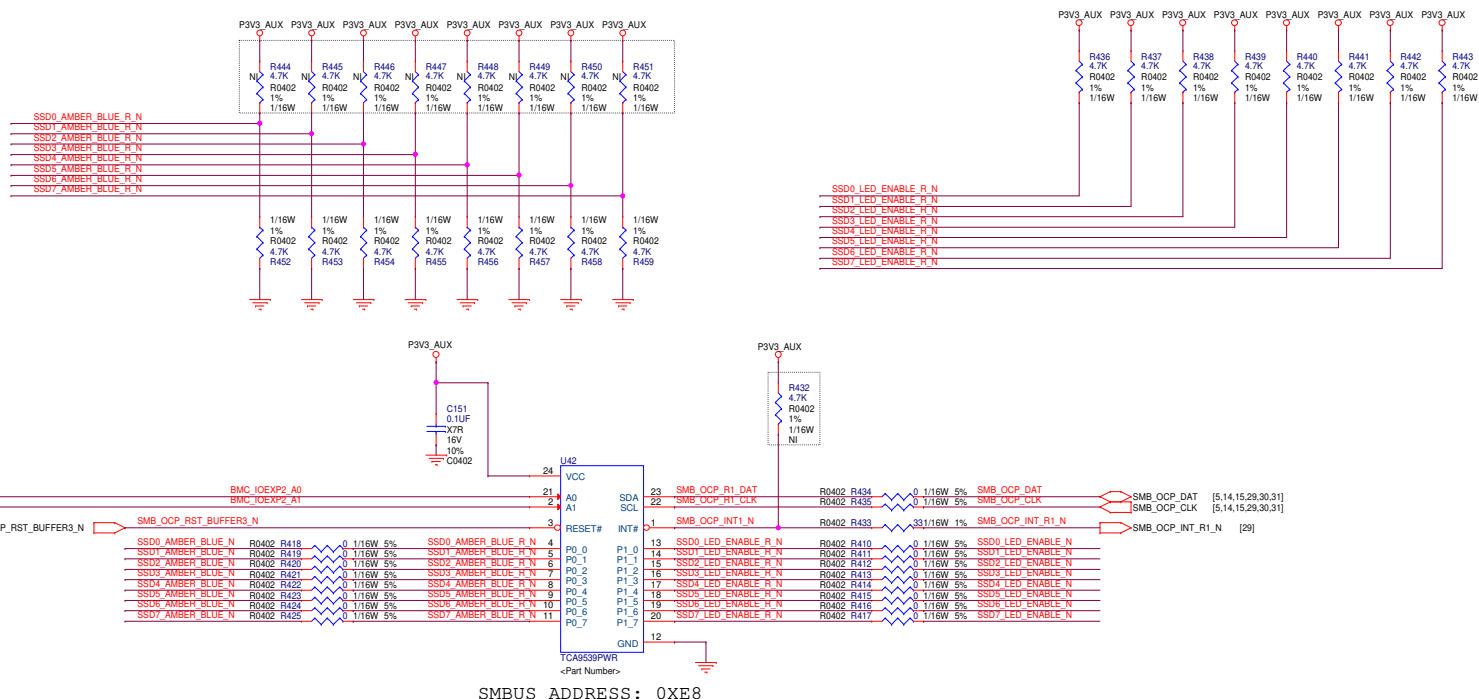
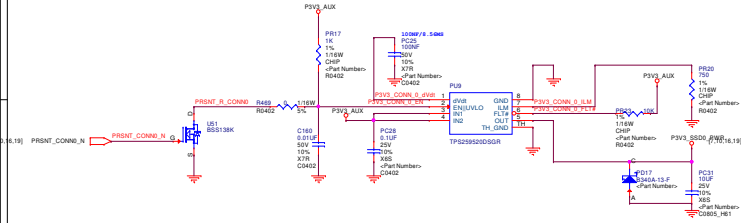


Figure 4. TCA9539 Address

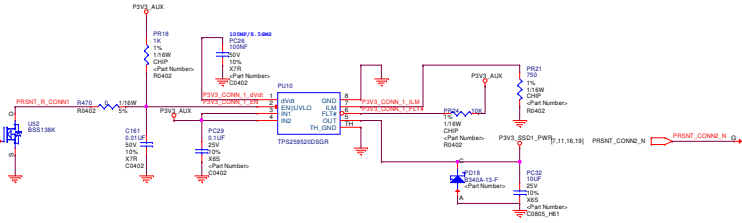
INPUTS		I ² C BUS SLAVE ADDRESS	
A1	A0		
L	L	116 (decimal), 74 (hexadecimal)	
L	H	117 (decimal), 75 (hexadecimal)	
H	L	118 (decimal), 76 (hexadecimal)	
H	H	119 (decimal), 77 (hexadecimal)	



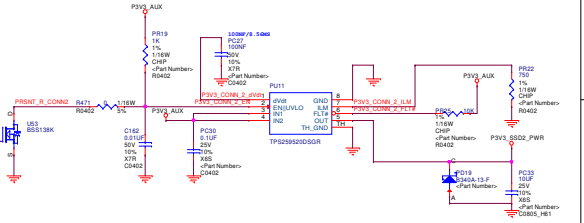
PWR for SSD0



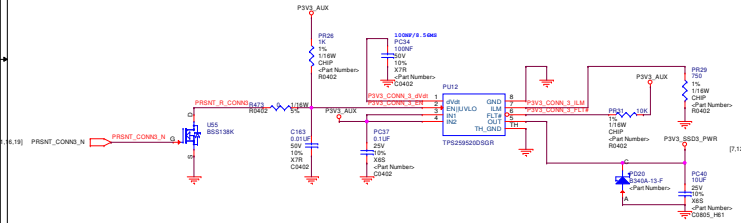
PWR for SSD1



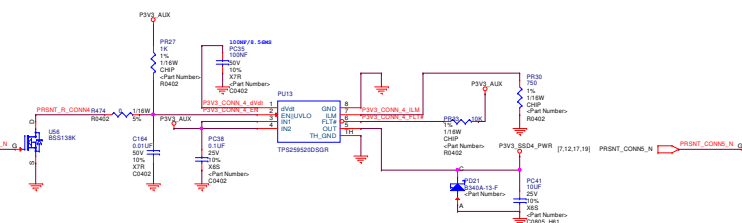
PWR for SSD2



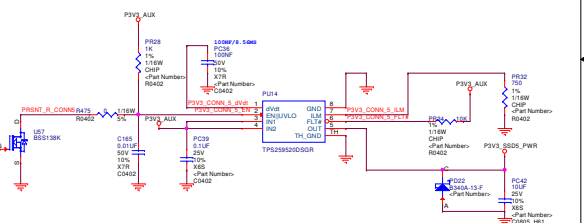
PWR for SSD3



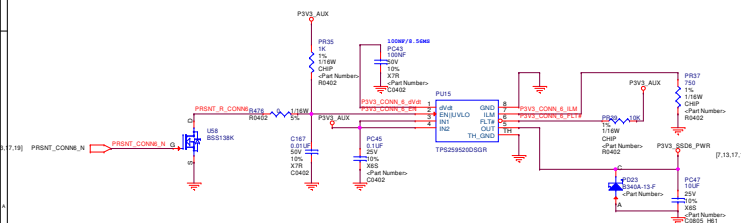
PWR for SSD4



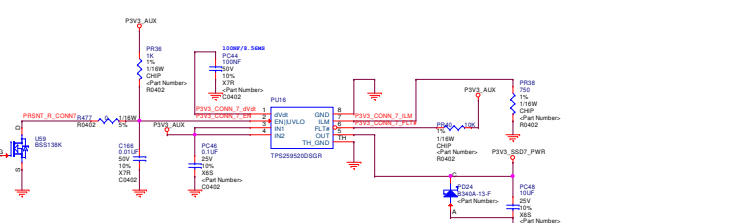
PWR for SSD5



PWR for SSD6

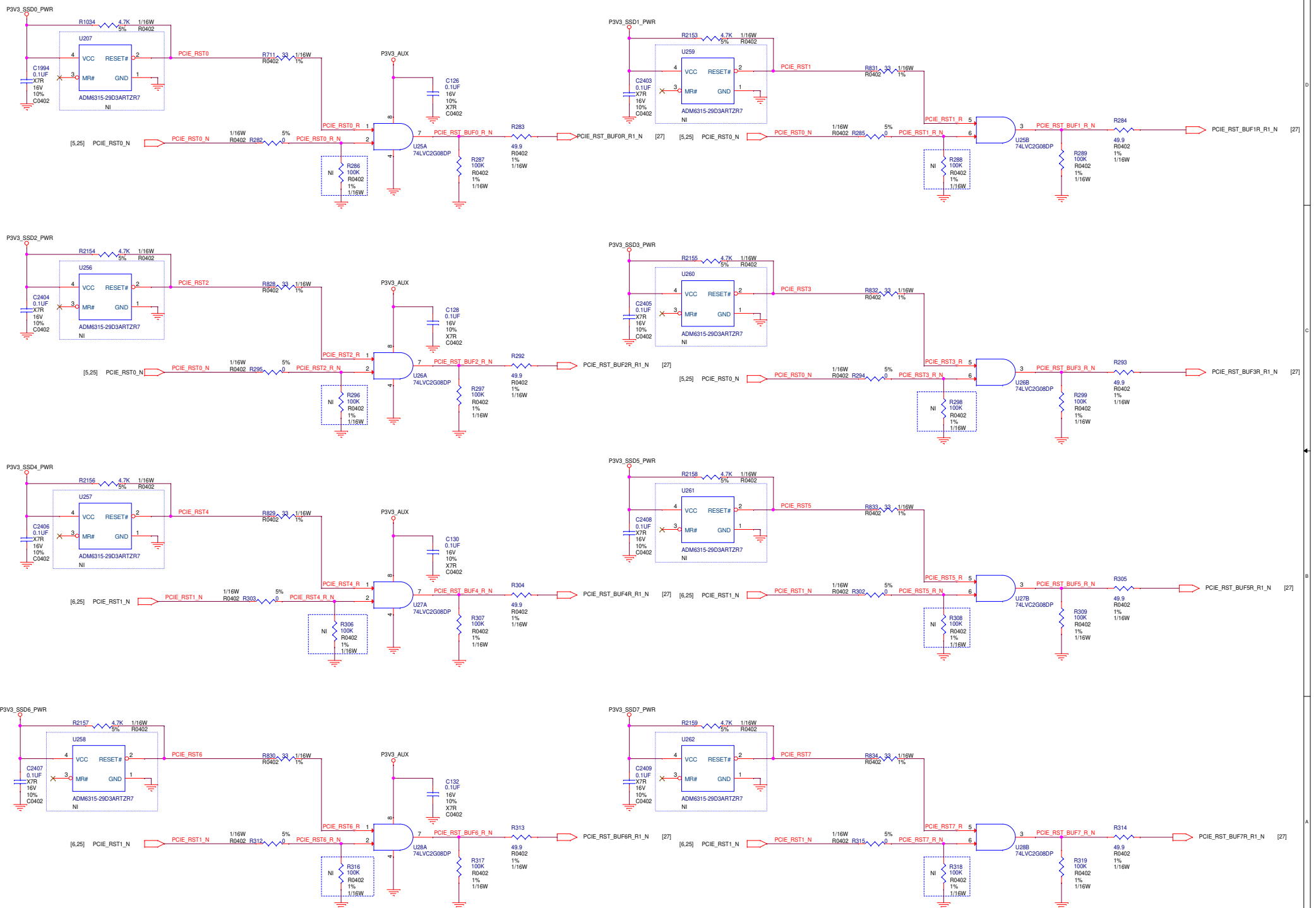


PWR for SSD7

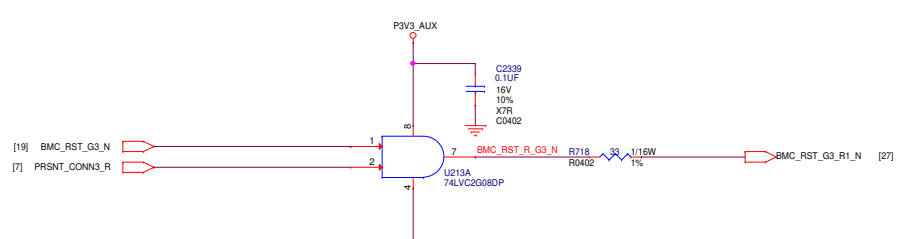
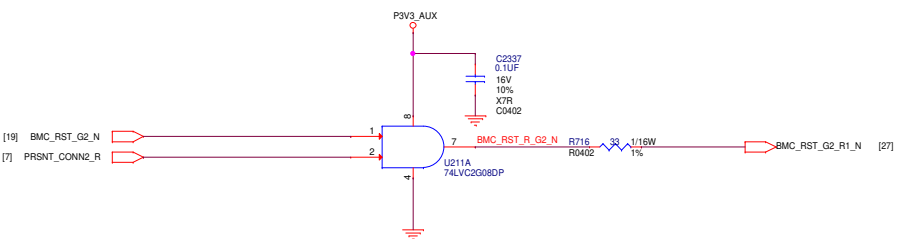
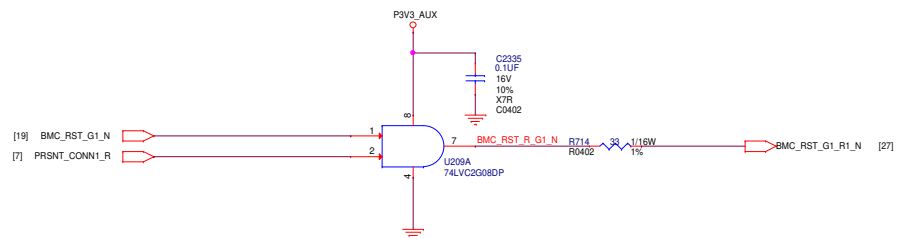
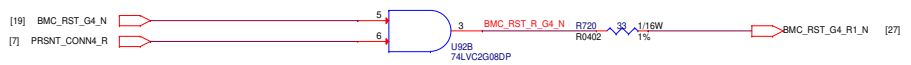
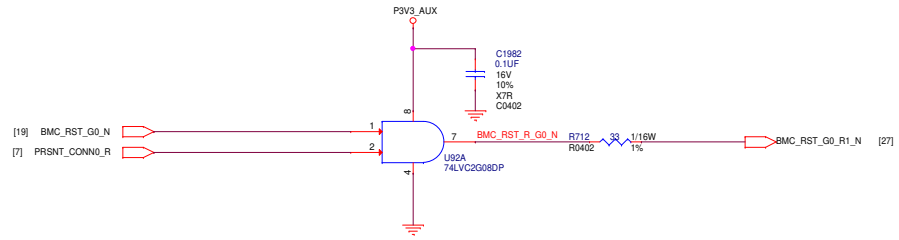


3.3V E-fuse

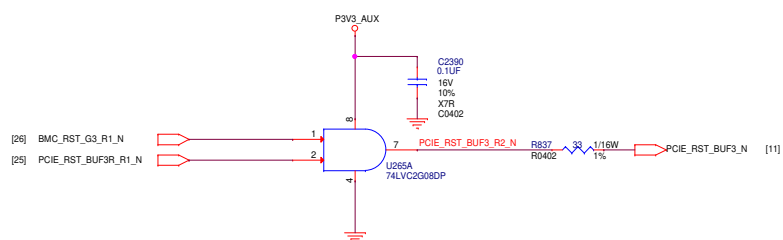
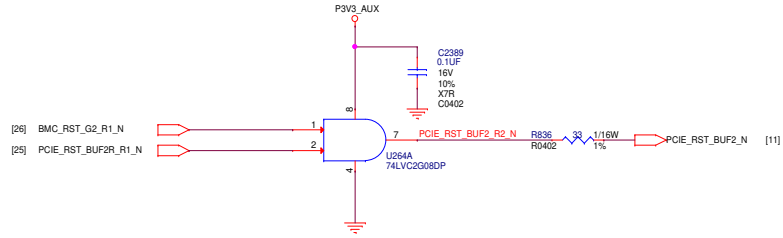
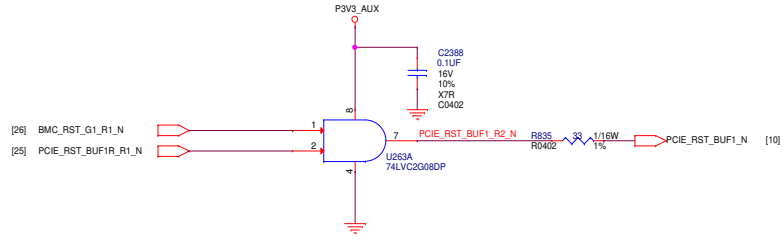
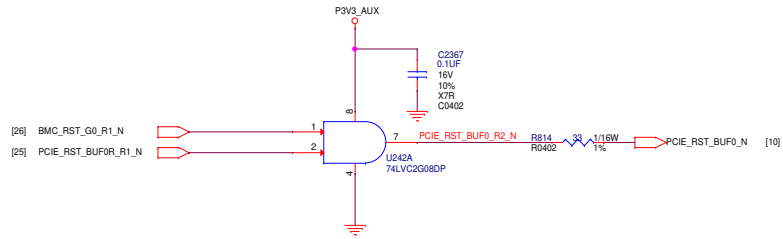
PCIE SSD RESET CIRCUIT



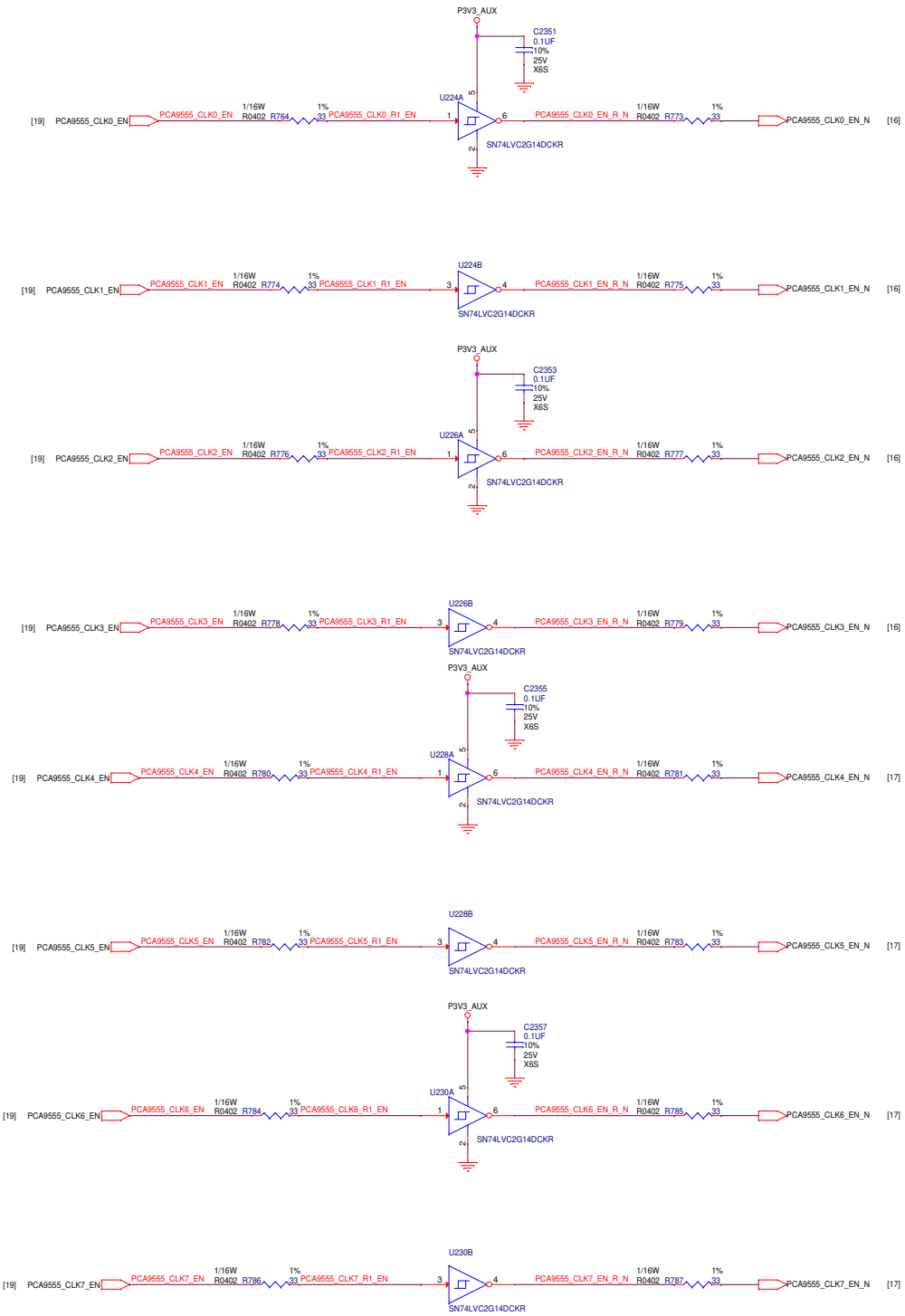
PCIE SSD RESET CIRCUIT



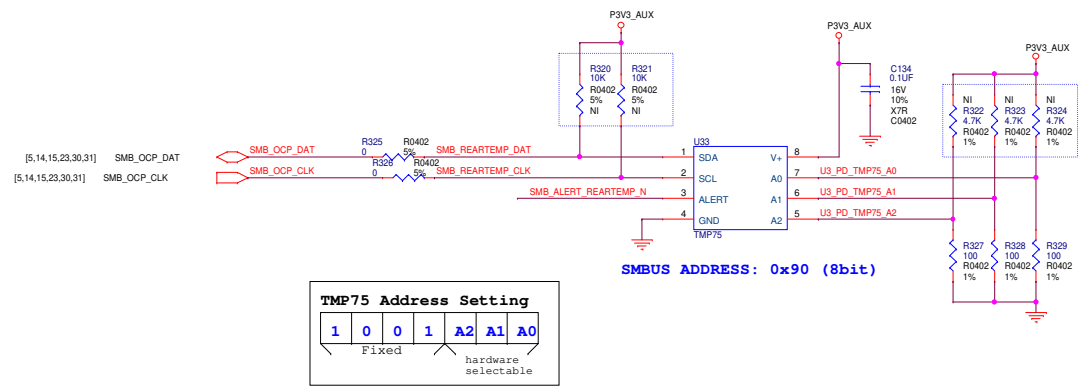
RESET CIRCUIT1



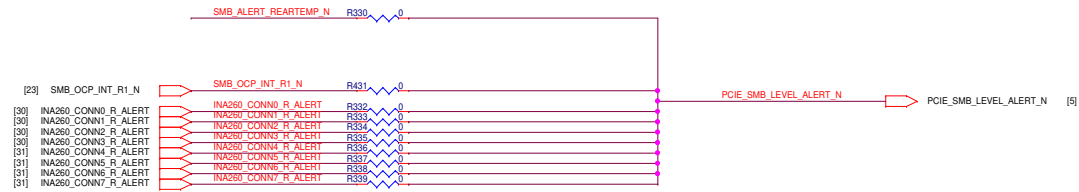
RESET CIRCUIT2



PCA955 CLOCK CIRCUIT



TMP75 Address Setting							
1	0	0	1	A2	A1	A0	
Fixed				hardware selectable			



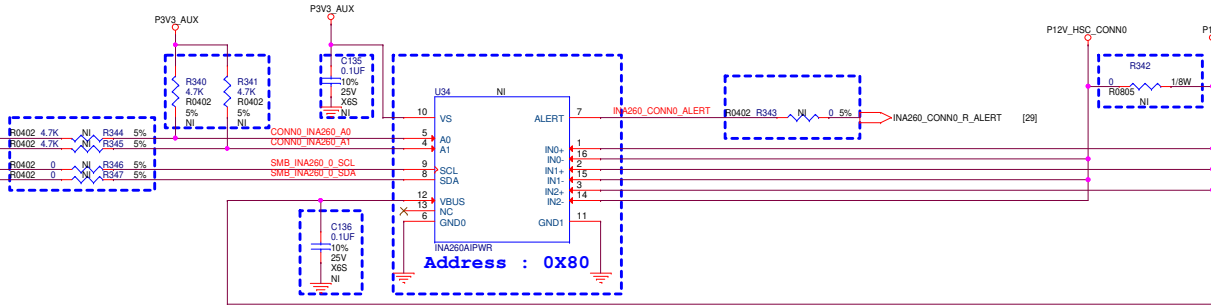
[23]	SMB_OCP_INT_R1_N	R431	0	PCIE_SMB_LEVEL_ALERT_N	[5]
[30]	INA260_CONN0_R_ALERT	R332	0		
[30]	INA260_CONN1_R_ALERT	R333	0		
[30]	INA260_CONN2_R_ALERT	R334	0		
[30]	INA260_CONN3_R_ALERT	R335	0		
[31]	INA260_CONN4_R_ALERT	R336	0		
[31]	INA260_CONN5_R_ALERT	R337	0		
[31]	INA260_CONN6_R_ALERT	R338	0		
[31]	INA260_CONN7_R_ALERT	R339	0		

Table 2. Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V5	1000001
GND	SDA	1000010
GND	SCL	1000011
V5	GND	1000100
V5	V5	1000101
V5	SDA	1000110
V5	SCL	1000111
SDA	GND	1001000
SDA	V5	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V5	1001101
SCL	SDA	1001110
SCL	SCL	1001111

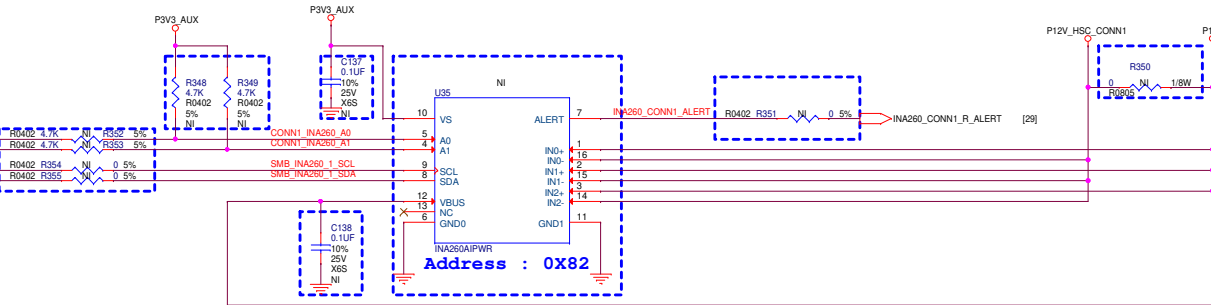
[5,14,15,23,29,30,31]
[5,14,15,23,29,30,31]

SMB_OCP_CLK
SMB_OCP_DAT



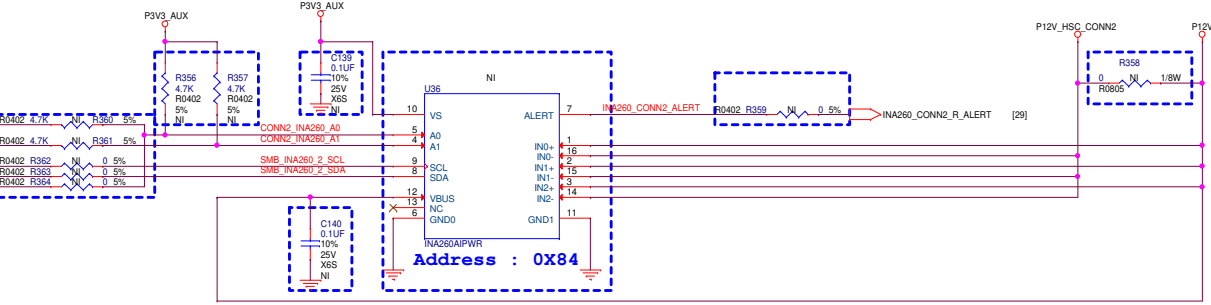
[5,14,15,23,29,30,31]
[5,14,15,23,29,30,31]

SMB_OCP_CLK
SMB_OCP_DAT



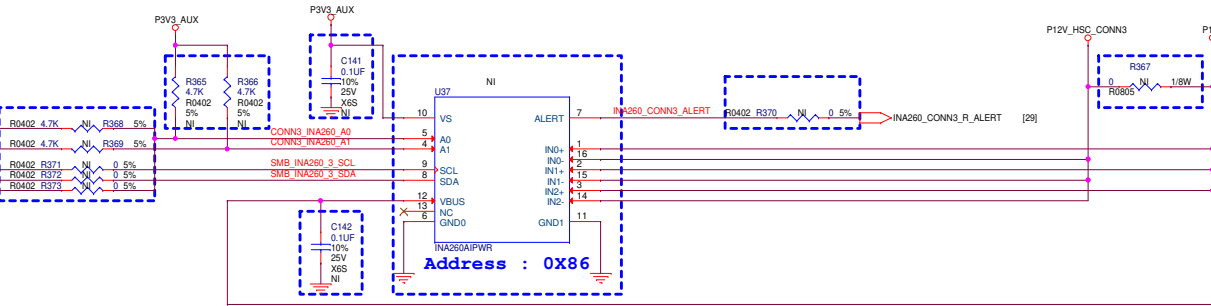
[5,14,15,23,29,30,31]
[5,14,15,23,29,30,31]

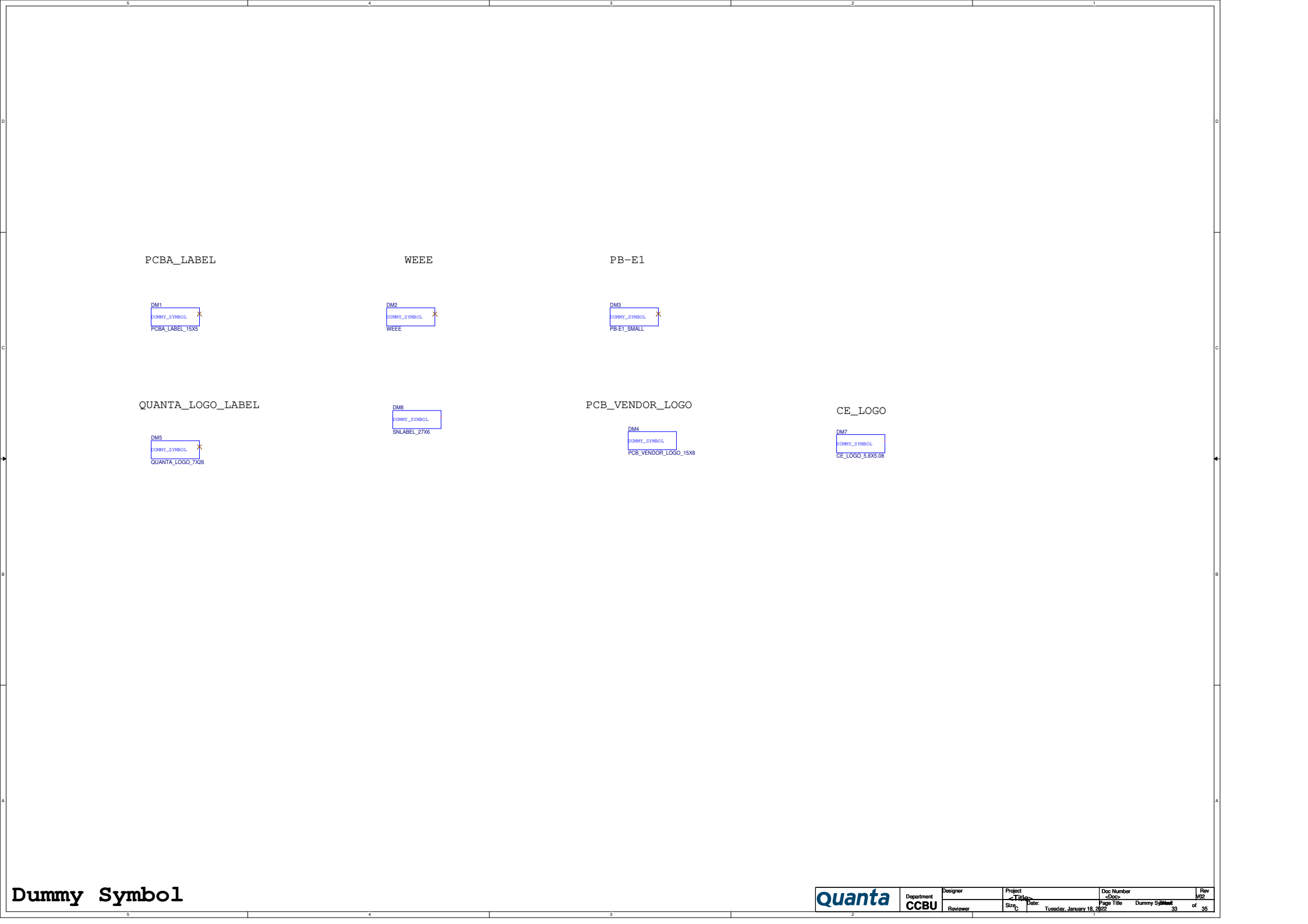
SMB_OCP_CLK
SMB_OCP_DAT



[5,14,15,23,29,30,31]
[5,14,15,23,29,30,31]

SMB_OCP_CLK
SMB_OCP_DAT





PCBA_LABEL

WEEE

PB-E1

DM1
DUMMY_SYMBOL
PCBA_LABEL_15X5

DM2
DUMMY_SYMBOL
WEEE

DM3
DUMMY_SYMBOL
PB-E1_SMALL

QUANTA_LOGO_LABEL

PCB_VENDOR_LOGO

CE_LOGO

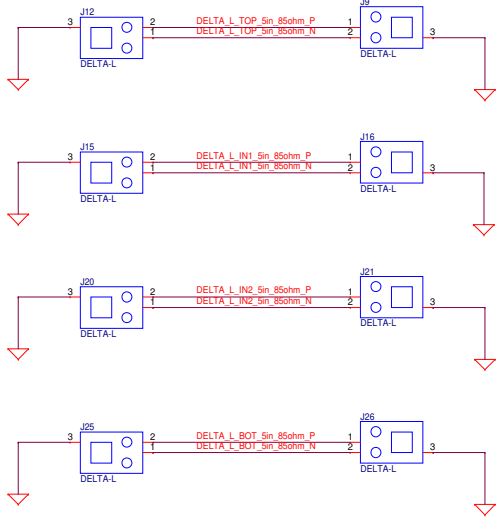
DM5
DUMMY_SYMBOL
QUANTA_LOGO_7X28

DM8
DUMMY_SYMBOL
SNLABEL_27X8

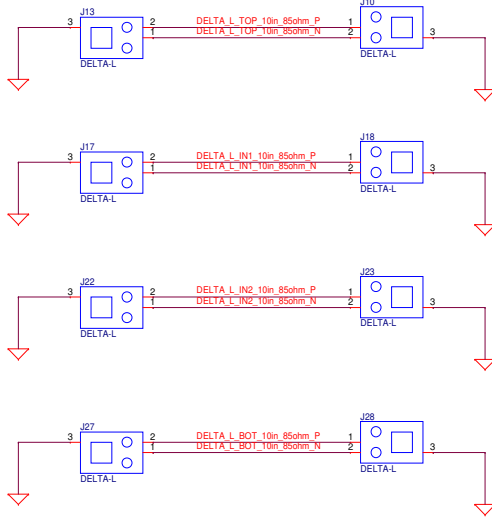
DM4
DUMMY_SYMBOL
PCB_VENDOR_LOGO_15X8

DM7
DUMMY_SYMBOL
CE_LOGO_5.8X5.08

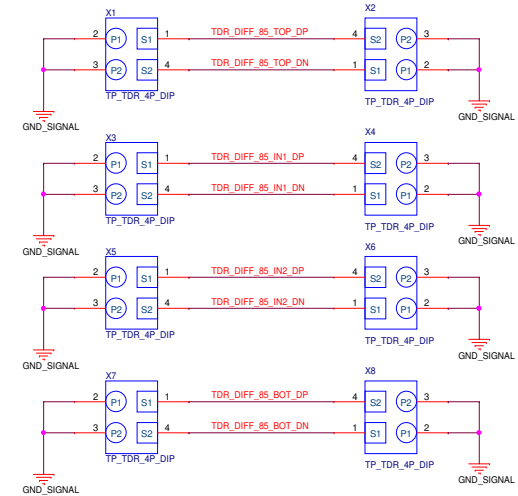
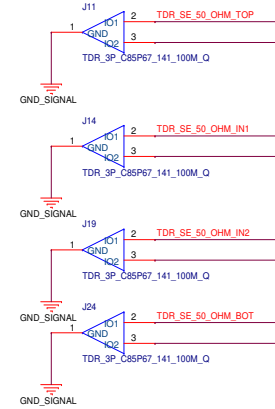
5 inch trace



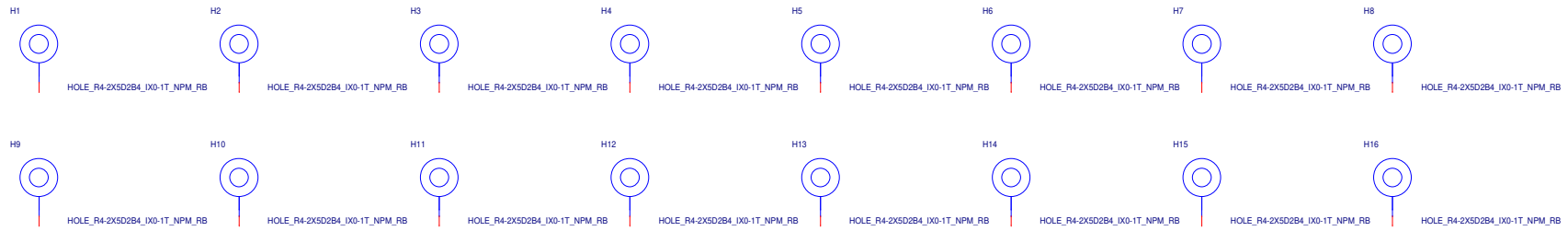
10 inch trace



TDR



SSD SCREW HOLE



Gourd HOLE

